

## SPDT SWITCH GaAs MMIC

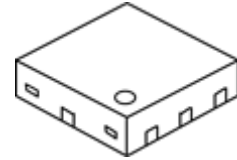
### ■ GENERAL DESCRIPTION

The NJG1806K75 is a 1bit control SPDT switch IC suited for switching transmit receive signals at WLAN application and receive signals at 3G/ LTE systems.

The NJG1806K75 features low insertion loss, high isolation, and high handling power down to 1.8V control voltage at high frequency up to 6GHz.

This switch has ESD protection devices to achieve excellent ESD performances. And the ultra small and ultra thin package of DFN6-75 is adopted.

### ■ PACKAGE OUTLINE



NJG1806K75

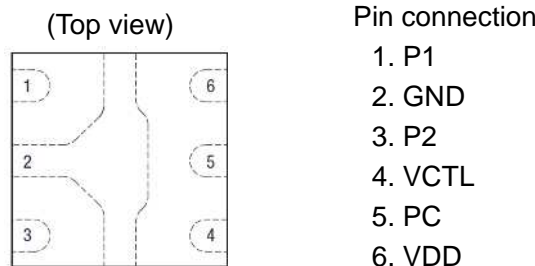
### ■ APPLICATION

- 802.11a/b/g/n/ac/ax networks and 3G/ LTE applications
- WLAN Module/ Repeaters, Cellular phone and others mobile device.

### ■ FEATURES

- Low control voltage  $V_{CTL(H)}=1.8V$  typ.
- Voltage operation  $V_{DD}=3.3V$  typ.
- Low insertion loss
  - 0.35dB typ. @f=0.7GHz
  - 0.35dB typ. @f=1.9GHz
  - 0.35dB typ. @f=2.4 to 2.5GHz
  - 0.40dB typ. @f=4.9 to 5.9GHz
- High isolation
  - 30dB typ. @f=0.7GHz
  - 25dB typ. @f=1.9GHz
  - 25dB typ. @f=2.4 to 2.5GHz
  - 25dB typ. @f=4.9 to 5.9GHz
- P-1dB  $P_{-1dB}=+31dBm$  typ. @0.7 to 5.9 GHz
- Ultra small & ultra thin package DFN6-75 (Package Size: 1.0x1.0x0.375mm typ.)
- RoHS compliant and Halogen Free, MSL1

### ■ PIN CONFIGURATION



### ■ TRUTH TABLE

“H”= $V_{CTL(H)}$ , “L”= $V_{CTL(L)}$

ON PATH	VCTL
PC-P1	H
PC-P2	L

NOTE: Please note that any data or drawing in this catalog is subject to change.

## ■ ABSOLUTE MAXIMUM RATINGS

$T_a=+25^{\circ}\text{C}$ ,  $Z_s=Z_l=50\Omega$

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNITS
RF Input Power	$P_{IN}$	$V_{DD}=3.3\text{V}$ , ON State Port	+31	dBm
Supply Voltage	$V_{DD}$		6.0	V
Control Voltage	$V_{CTL}$		6.0	V
Power Dissipation	$P_D$	4-layer FR4 PCB with through-hole (76.2x114.3mm), $T_j=150^{\circ}\text{C}$	380	mW
Operating Temperature	$T_{opr}$		-40 to +105	$^{\circ}\text{C}$
Storage Temperature	$T_{stg}$		-55 to +150	$^{\circ}\text{C}$

## ■ ELECTRICAL CHARACTERISTICS1 (DC CHARACTERISTICS)

(General conditions:  $T_a=+25^{\circ}\text{C}$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{DD}$		2.5	3.3	5.0	V
Operating Current	$I_{DD}$	No RF input, $V_{DD}=3.3\text{V}$	-	15	30	$\mu\text{A}$
Control Voltage (HIGH)	$V_{CTL(H)}$		1.35	1.8	5.0	V
Control Voltage (LOW)	$V_{CTL(L)}$		0	-	0.45	V
Control Current	$I_{CTL}$	$V_{CTL(H)}=1.8\text{V}$	-	3	10	$\mu\text{A}$

## ■ ELECTRICAL CHARACTERISTICS2 (RF CHARACTERISTICS)

(General conditions:  $V_{DD}=3.3V$ ,  $V_{CTL(H)}=1.8V$ ,  $V_{CTL(L)}=0V$ ,  $T_a=+25^{\circ}C$ ,  $Z_S=Z_I=50\Omega$ , with application circuit)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion loss 1	LOSS1	f=0.7GHz	-	0.35	0.55	dB
Insertion loss 2	LOSS2	f=1.9GHz,	-	0.35	0.55	dB
Insertion loss 3	LOSS3	f=2.4 to 2.5GHz	-	0.35	0.55	dB
Insertion loss 4	LOSS4	f=4.9 to 5.9GHz	-	0.40	0.60	dB
Isolation 1	ISL1	f=0.7GHz	28	30	-	dB
Isolation 2	ISL2	f=1.9GHz	23	25	-	dB
Isolation 3	ISL3	f=2.4 to 2.5GHz	23	25	-	dB
Isolation 4	ISL4	f=4.9 to 5.9GHz	23	25	-	dB
Return loss 1	RL1	f=0.7GHz	15	20	-	dB
Return loss 2	RL2	f=1.9GHz	18	28	-	dB
Return loss 3	RL3	f=2.4 to 2.5GHz	18	28	-	dB
Return loss 4	RL4	f=4.9 to 5.9GHz	15	20	-	dB
Input power at 1dB compression point	$P_{-1dB}$	f=0.7 to 5.9GHz	+28	+31	-	dBm
Switching time	$T_{SW}$	50% $V_{CTL}$ to 10%/90% RF	-	150	300	ns

## ■ TERMINAL INFORMATION

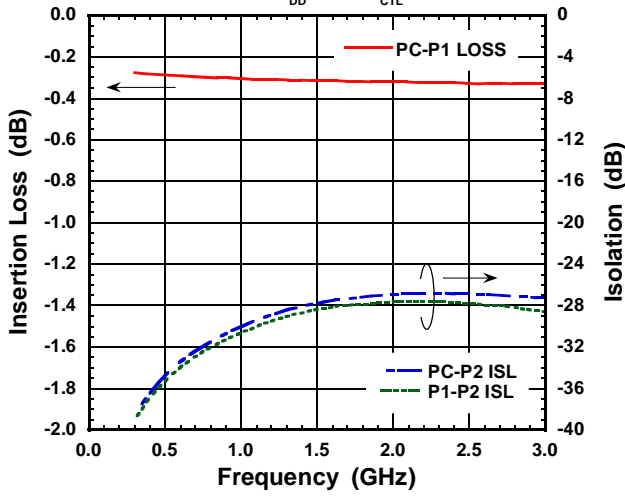
No.	SYMBOL	DESCRIPTION
1	P1	RF terminal. An external DC blocking capacitor is required.
2	GND	Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance.
3	P2	RF terminal. An external DC blocking capacitor is required.
4	VCTL	Control voltage input terminal. This terminal is set to High-Level (+1.35 to +5.0V) or Low-Level (0 to +0.45V).
5	PC	Common RF terminal. An external DC blocking capacitor is required.
6	VDD	Positive voltage supply terminal. The positive voltage (+2.5 to +5.0V) has to be supplied. Please connect a bypass capacitor with GND terminal for excellent RF performance.

## ■ ELECTRICAL CHARACTERISTICS

General conditions:  $V_{DD}=3.3V$ ,  $V_{CTL}=1.8/0V$ ,  $f=0.7$  to  $2.0GHz$ ,  $T_a=+25^\circ C$ ,  $Z_S=Z_L=50\Omega$ , with application circuit

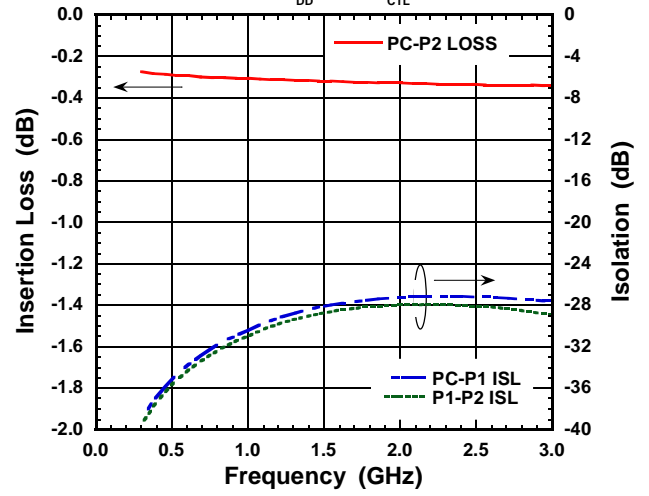
### Loss, ISL vs Frequency

(PC-P1 ON,  $V_{DD}=3.3V$ ,  $V_{CTL}=1.8V$ )



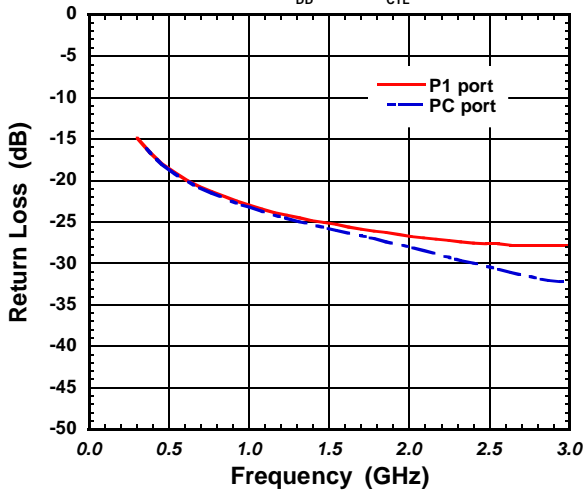
### Loss, ISL vs Frequency

(PC-P2 ON,  $V_{DD}=3.3V$ ,  $V_{CTL}=0V$ )



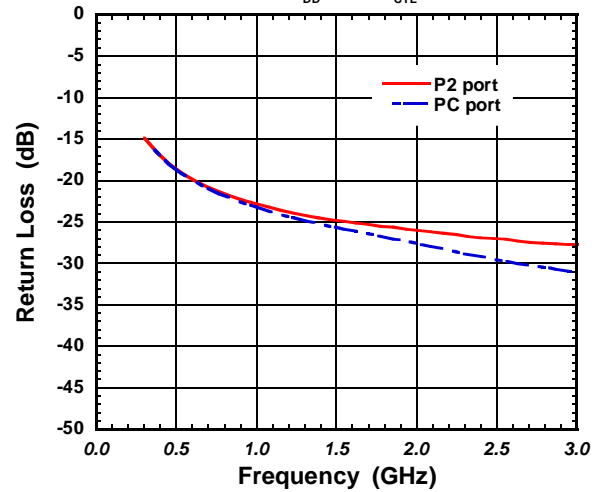
### Return Loss vs Frequency

(PC-P1 ON,  $V_{DD}=3.3V$ ,  $V_{CTL}=1.8V$ )



### Return Loss vs Frequency

(PC-P2 ON,  $V_{DD}=3.3V$ ,  $V_{CTL}=0V$ )

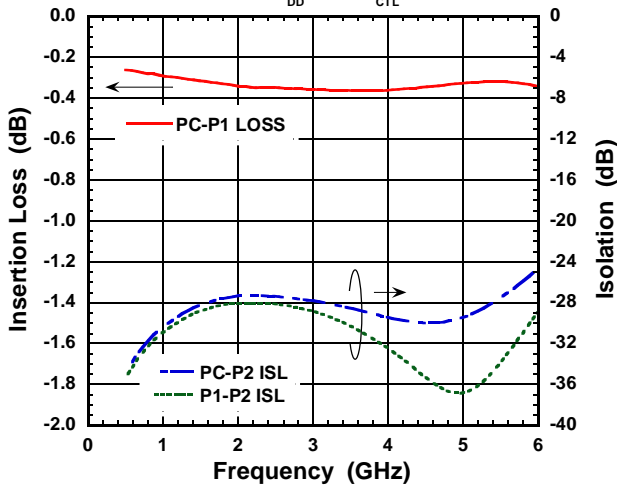


## ■ ELECTRICAL CHARACTERISTICS

General conditions:  $V_{DD}=3.3V$ ,  $V_{CTL}=1.8/0V$ ,  $f=2.0$  to  $5.9GHz$ ,  $T_a=+25^\circ C$ ,  $Z_S=Z_L=50\Omega$ , with application circuit

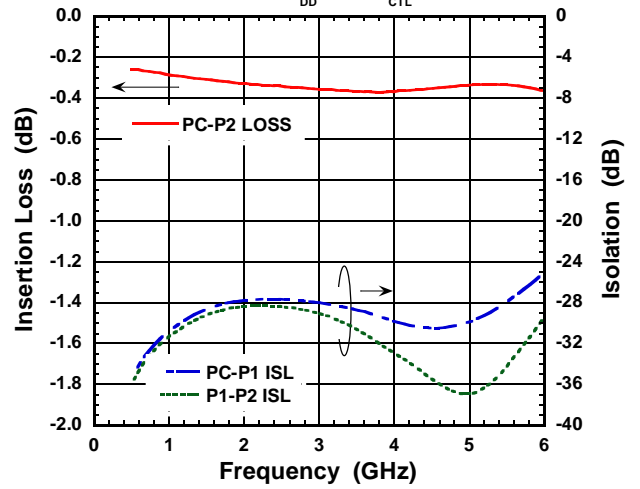
### Loss, ISL vs Frequency

(PC-P1 ON,  $V_{DD}=3.3V$ ,  $V_{CTL}=1.8V$ )



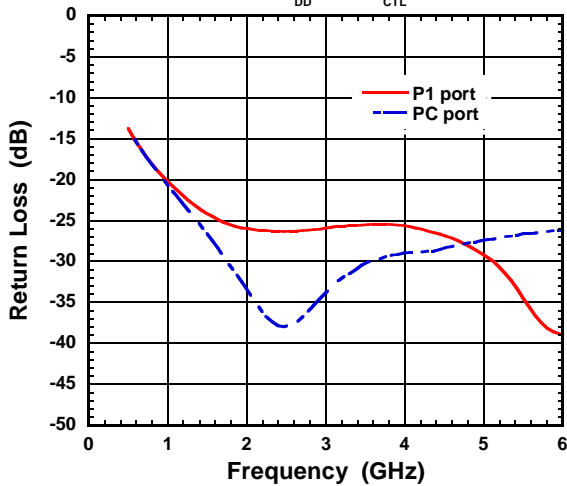
### Loss, ISL vs Frequency

(PC-P2 ON,  $V_{DD}=3.3V$ ,  $V_{CTL}=0V$ )



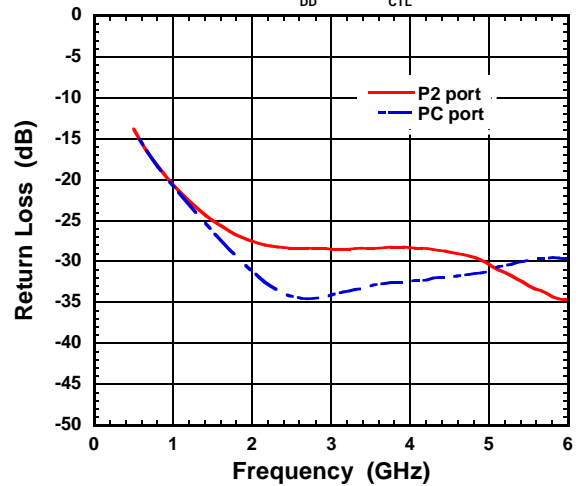
### Return Loss vs Frequency

(PC-P1 ON,  $V_{DD}=3.3V$ ,  $V_{CTL}=1.8V$ )



### Return Loss vs Frequency

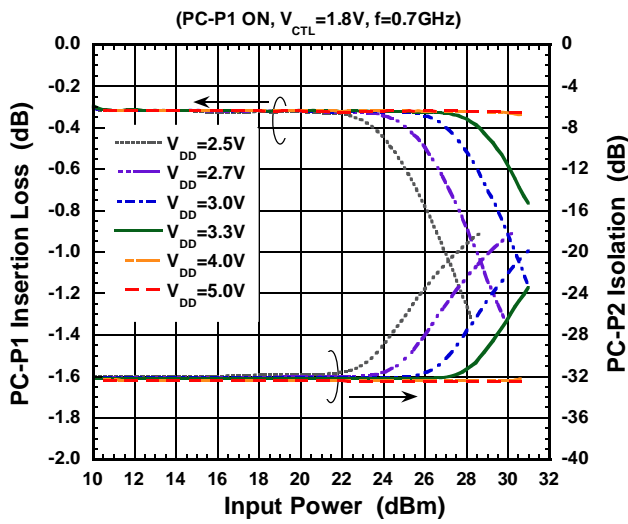
(PC-P2 ON,  $V_{DD}=3.3V$ ,  $V_{CTL}=0V$ )



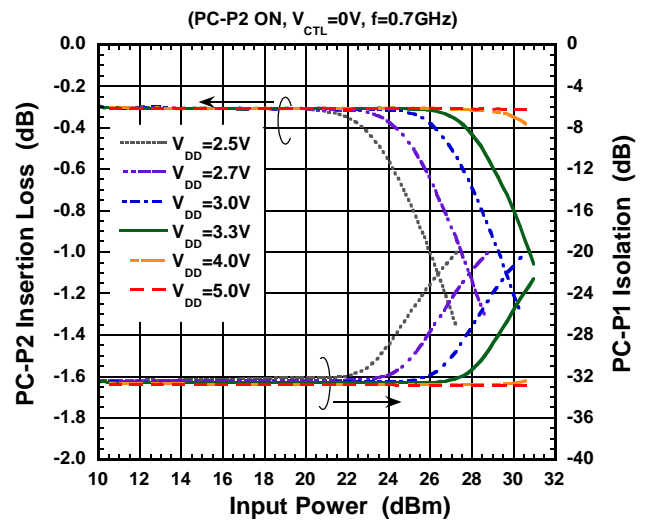
## ■ ELECTRICAL CHARACTERISTICS

General conditions:  $V_{DD}=3.3V$ ,  $V_{CTL}=1.8/0V$ ,  $T_a=+25^\circ C$ ,  $Z_S=Z_I=50\Omega$ , with application circuit

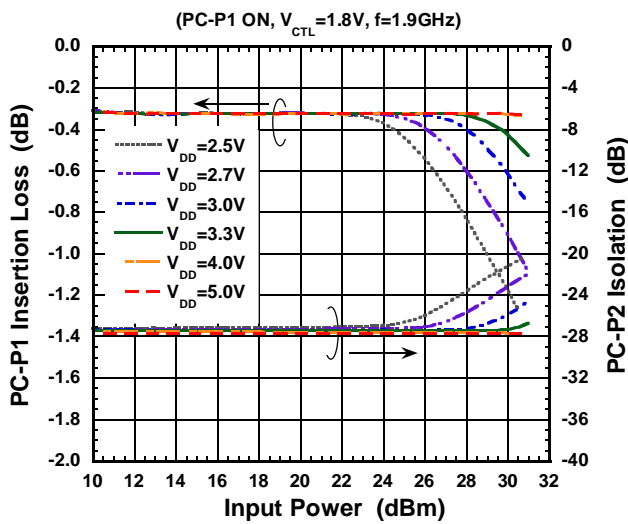
### Loss, ISL vs Input Power



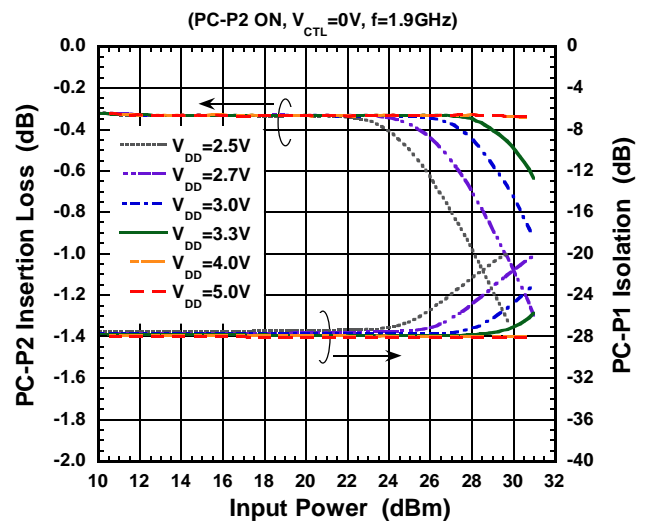
### Loss, ISL vs Input Power



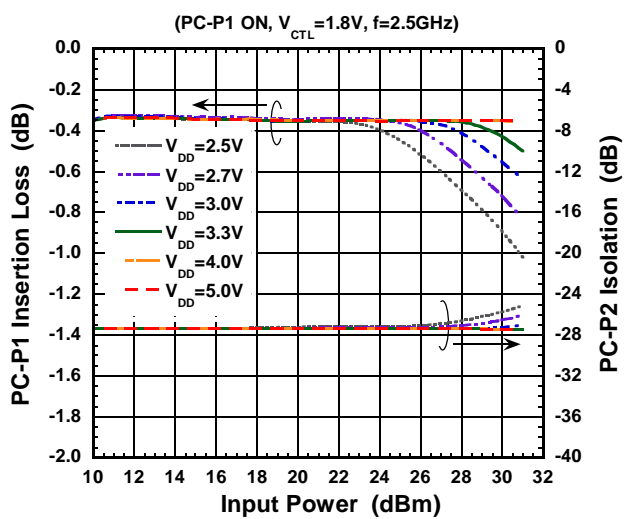
### Loss, ISL vs Input Power



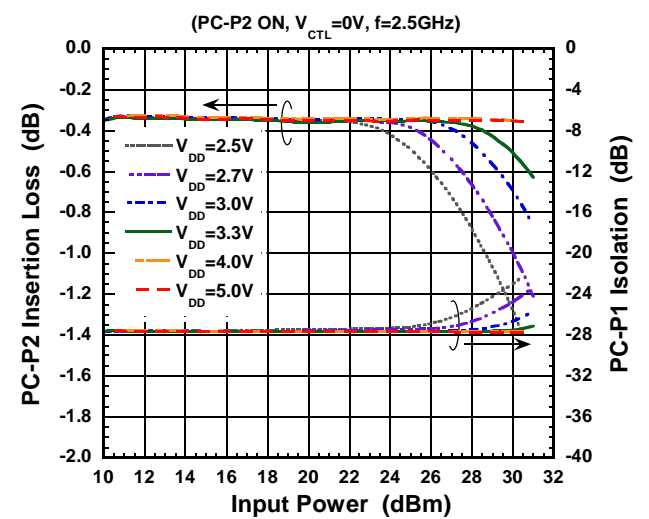
### Loss, ISL vs Input Power



### Loss, ISL vs Input Power



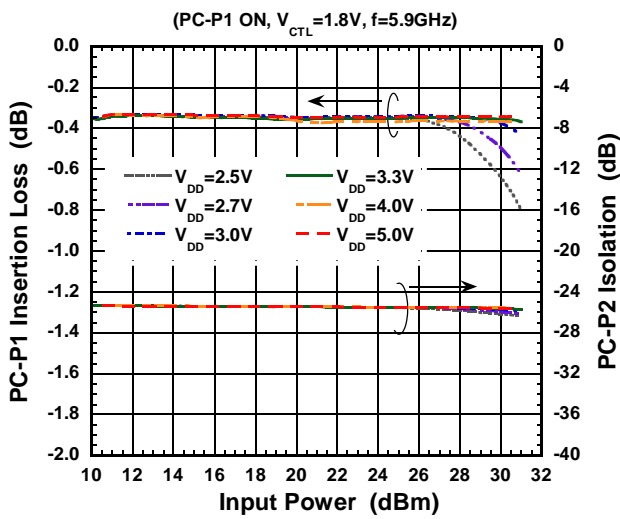
### Loss, ISL vs Input Power



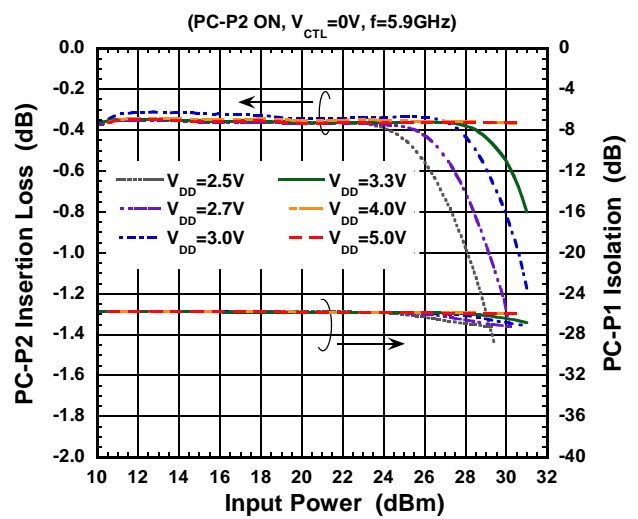
## ■ ELECTRICAL CHARACTERISTICS

General conditions:  $V_{DD}=3.3V$ ,  $V_{CTL}=1.8/0V$ ,  $T_a=+25^\circ C$ ,  $Z_S=Z_I=50\Omega$ , with application circuit

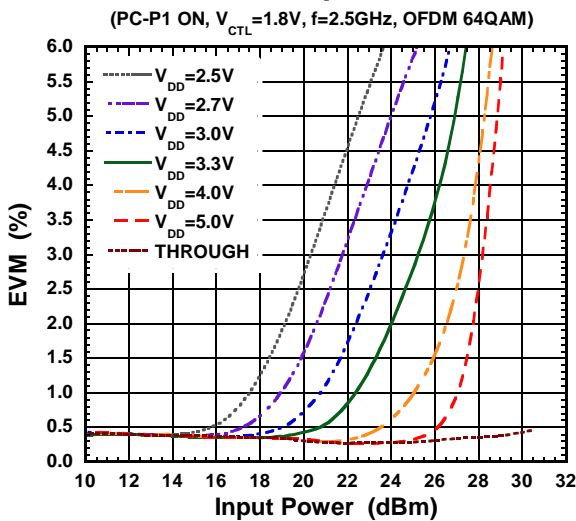
### Loss, ISL vs Input Power



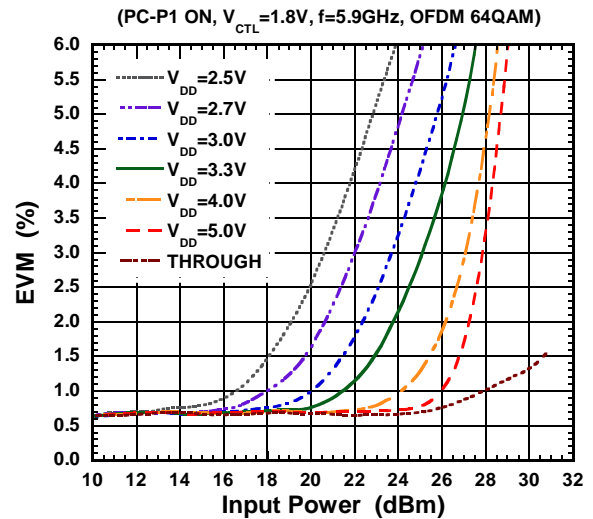
### Loss, ISL vs Input Power



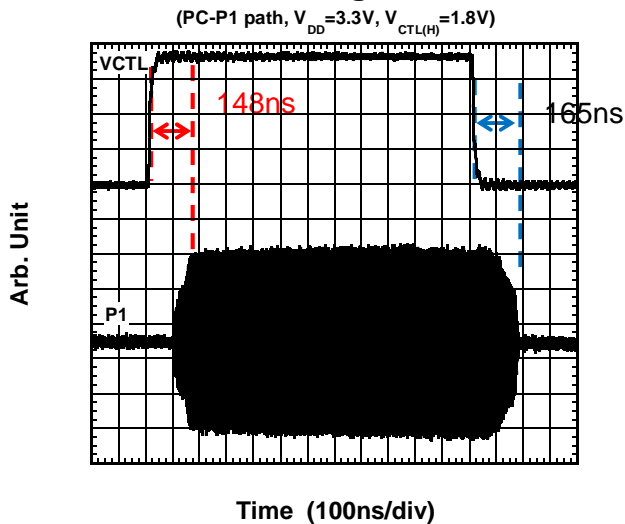
### EVM vs Input Power



### EVM vs Input Power



### Switching Time

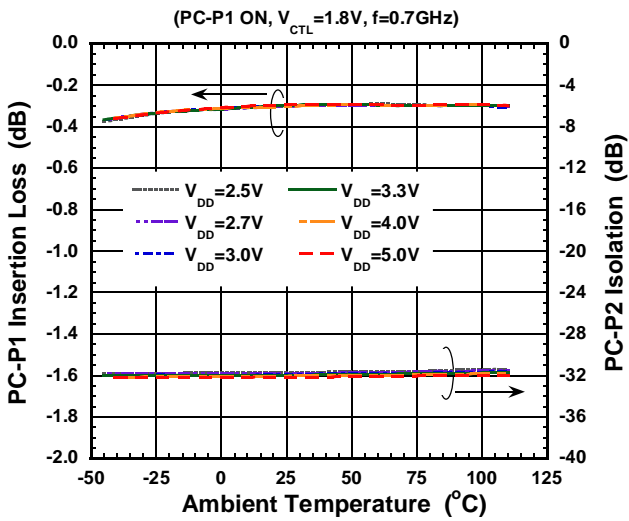




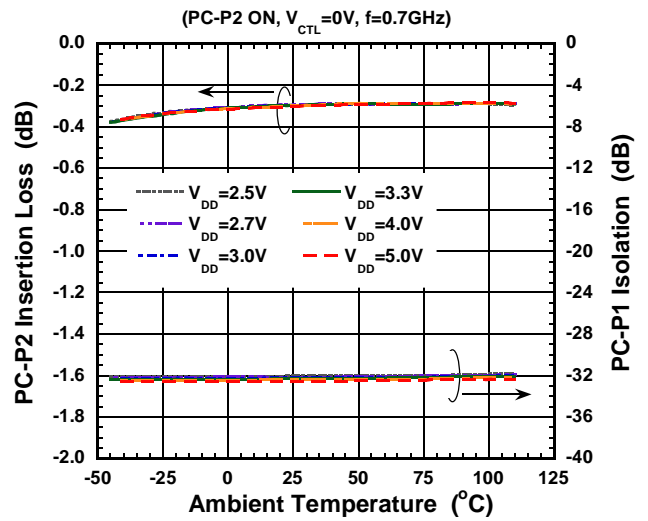
## ELECTRICAL CHARACTERISTICS

General conditions:  $V_{DD}=3.3V$ ,  $V_{CTL}=1.8/0V$ ,  $Z_S=Z_I=50\Omega$ , with application circuit

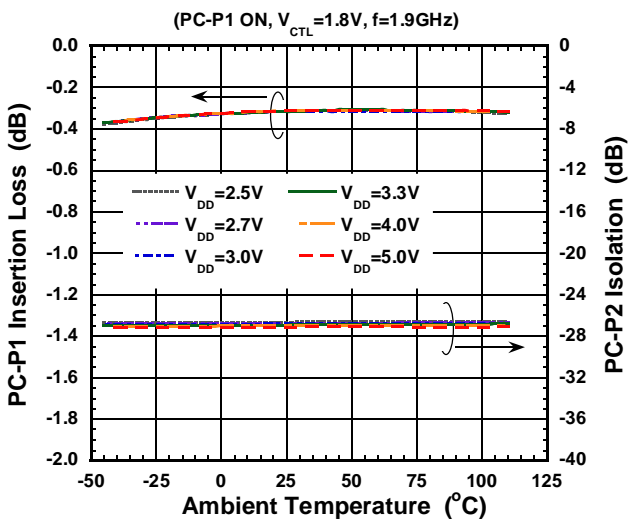
### Loss, ISL vs Temperature



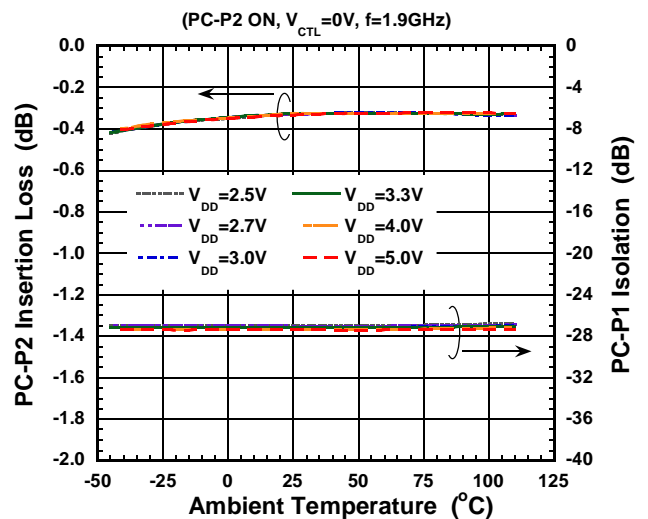
### Loss, ISL vs Temperature



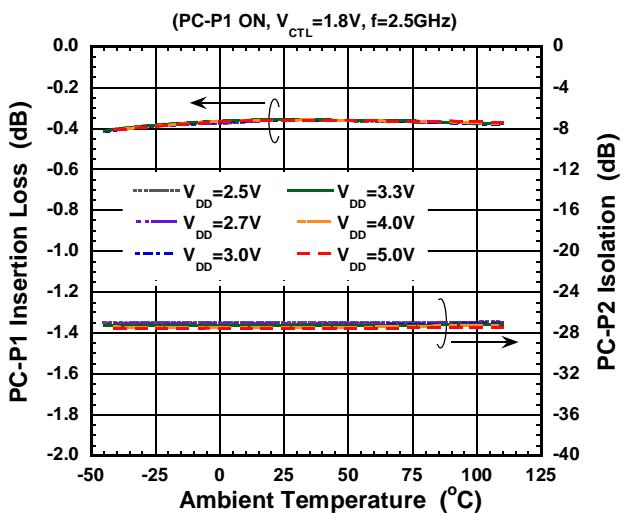
### Loss, ISL vs Temperature



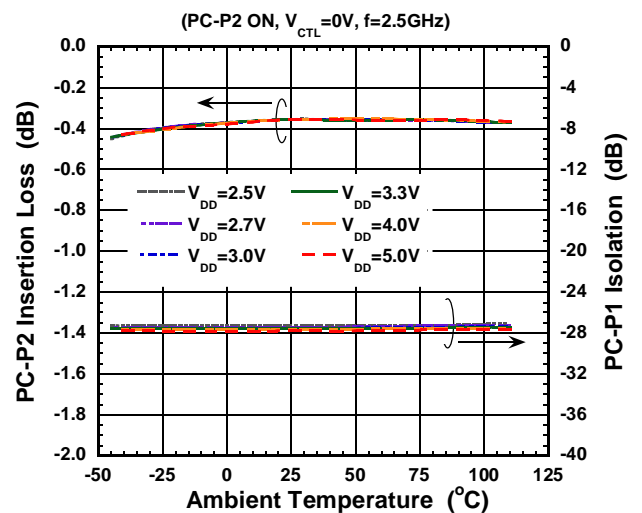
### Loss, ISL vs Temperature



### Loss, ISL vs Temperature



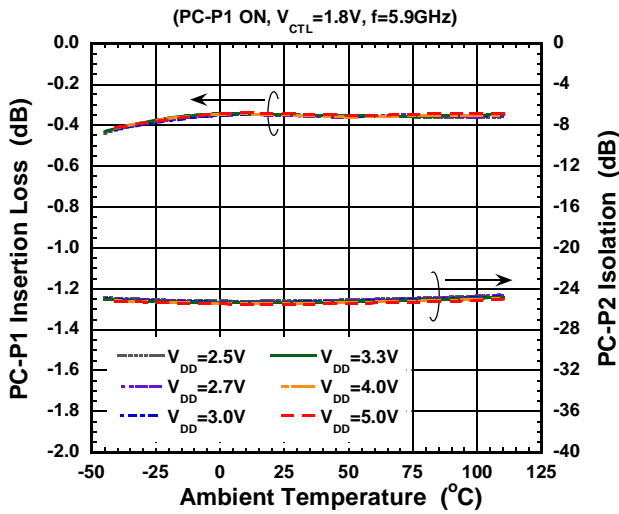
### Loss, ISL vs Temperature



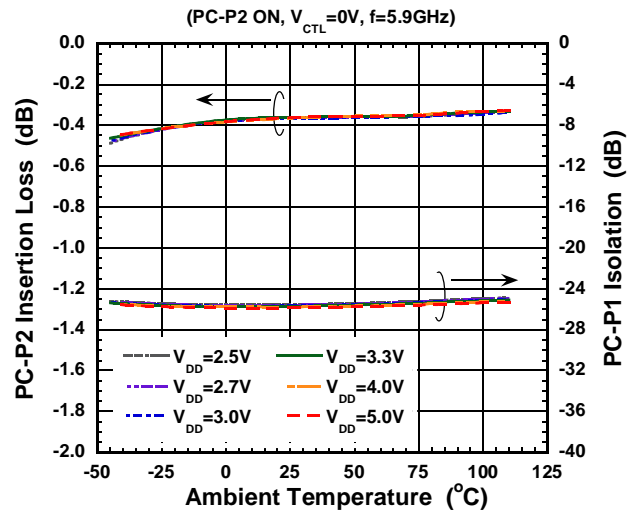
## ELECTRICAL CHARACTERISTICS

General conditions:  $V_{DD}=3.3V$ ,  $V_{CTL}=1.8/0V$ ,  $Z_S=Z_I=50\Omega$ , with application circuit

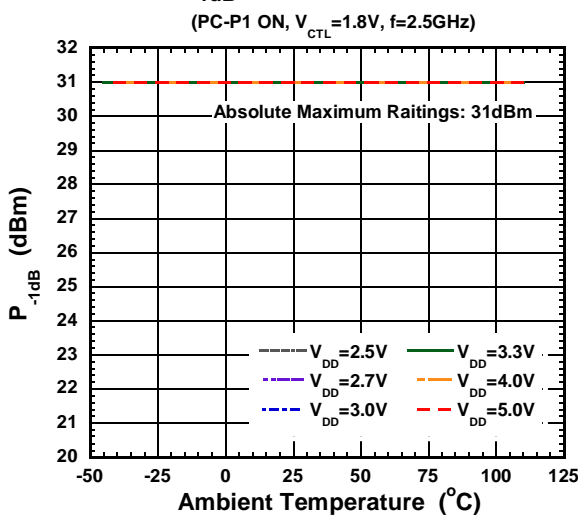
### Loss, ISL vs Temperature



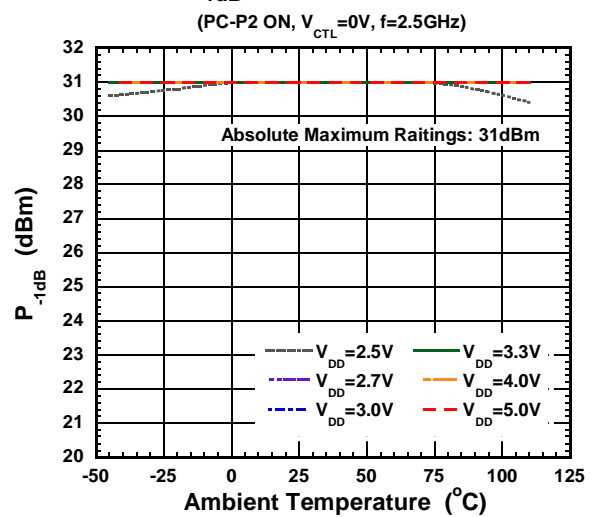
### Loss, ISL vs Temperature



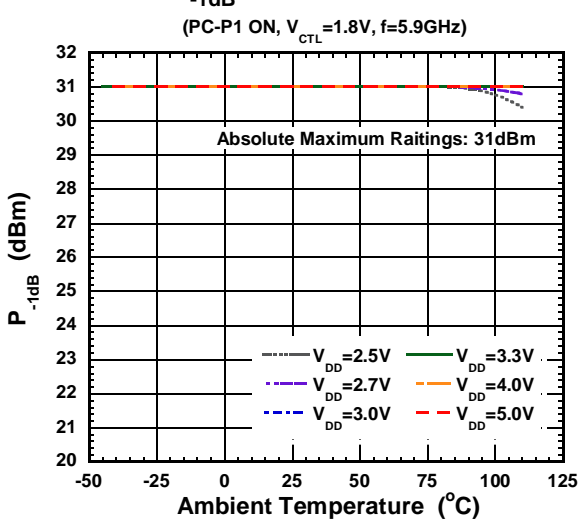
### $P_{-1dB}$ vs Temperature



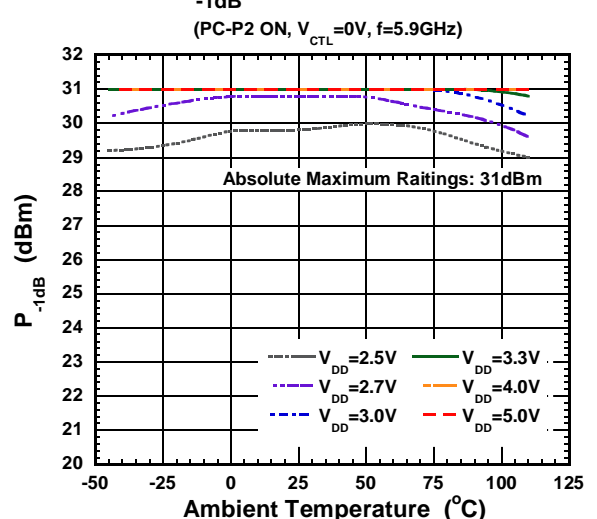
### $P_{-1dB}$ vs Temperature



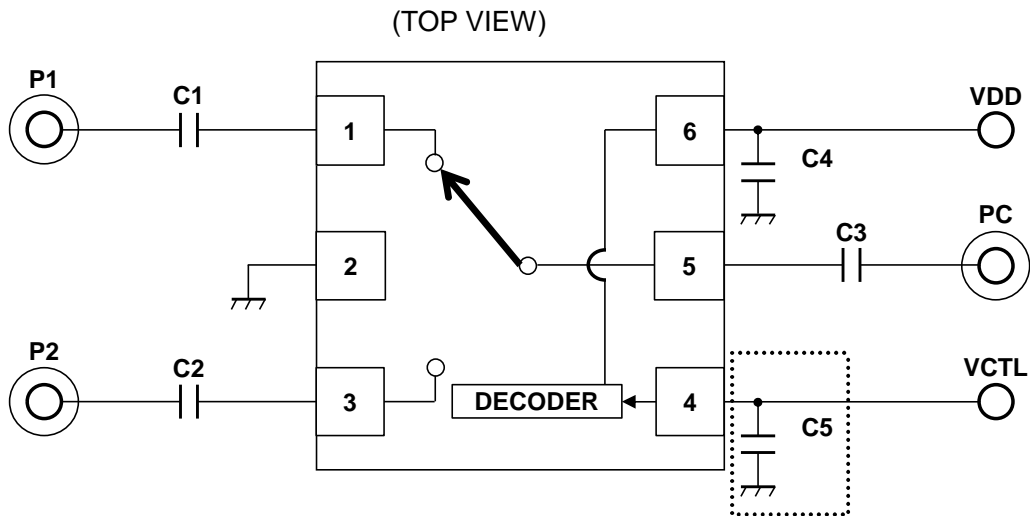
### $P_{-1dB}$ vs Temperature



### $P_{-1dB}$ vs Temperature



## APPLICATION CIRCUIT



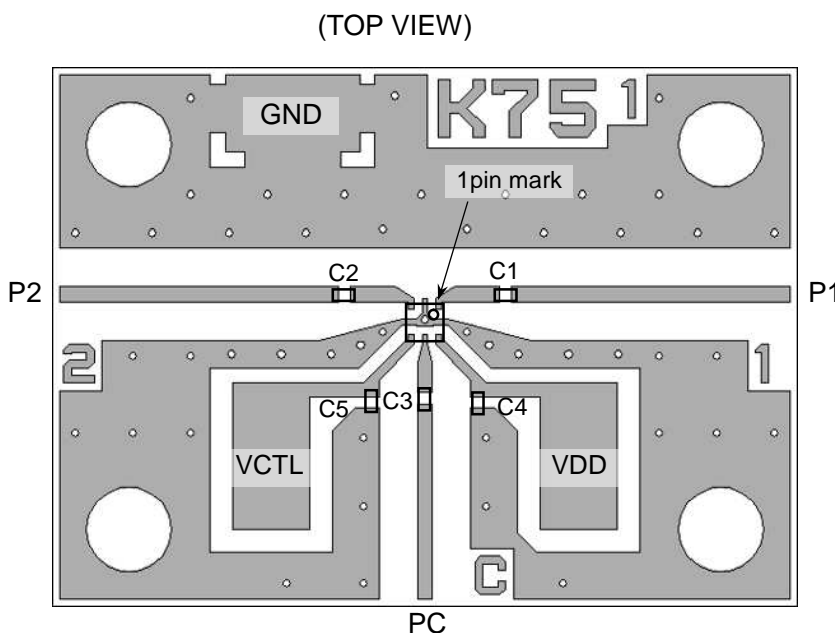
### NOTE:

The bypass capacitor, C5 is optional, and is recommended only when the control line is affected under noisy environment.

## PARTS LIST

Parts No.	Value		Notes
	Frequency range 0.7 ~ 2.0GHz	Frequency range 2.0 ~ 5.9GHz	
C1 to C3	56pF	27pF	Murata MFG (GRM03 series)
C4	1000pF	1000pF	
C5	10pF	10pF	

## RECOMMENDED PCB DESIGN

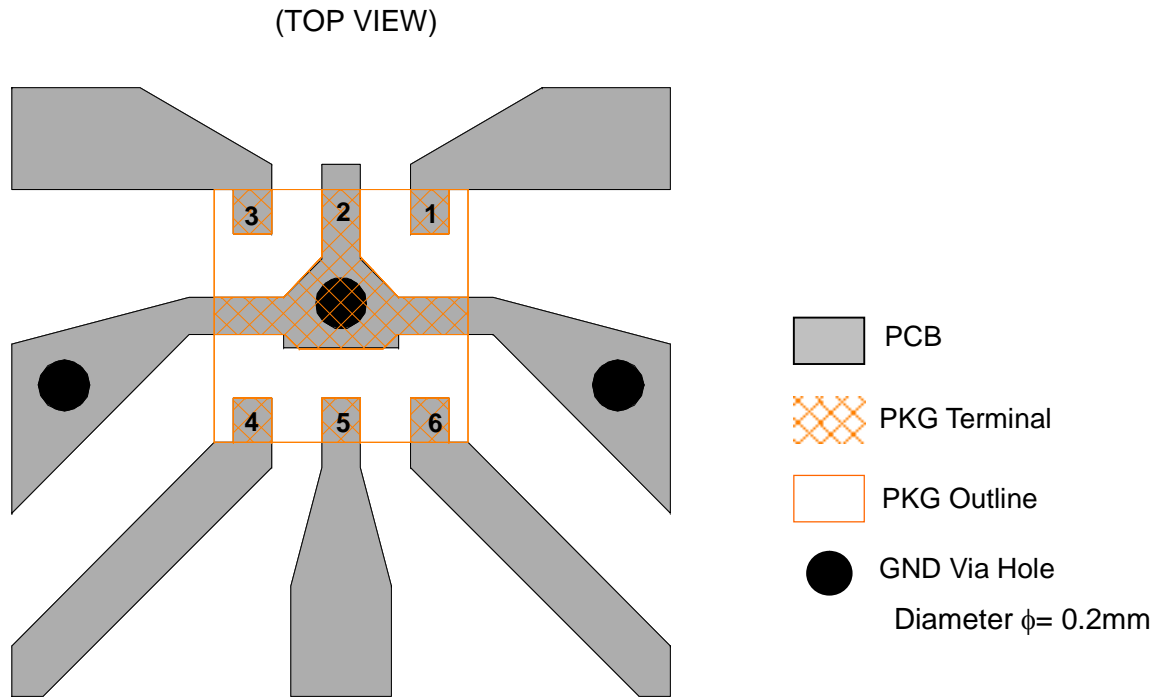


PCB: FR-4, t=0.2mm  
 Capacitor Size: 0603 (0.6 x 0.3 mm)  
 Strip Line Width: 0.4mm  
 PCB Size: 19.4 x 14.0mm  
 Through Hole Diameter: 0.2mm

### Loss of PCB, capacitor and connectors

Frequency (GHz)	Loss (dB)
0.7	0.15
1.9	0.26
2.4	0.30
2.5	0.31
4.9	0.59
5.9	0.71

## ■ PCB LAYOUT GUIDELINE



## PRECAUTIONS

- [1] The DC blocking capacitors should be placed at RF terminals. Please choose appropriate capacitance value at the application frequency.
- [2] For good RF performance, exposed pad should be connected to PCB ground plane as close as possible.


## RECOMMENDED FOOTPRINT PATTERN (6pin DFN Package 1.0x1.0mm) <Reference>

Package: 1.0mm x 1.0mm

Pin pitch: 0.35mm

 : Land

 : Mask (Open area) \*Metal mask thickness: 100μm

 : Resist (Open area)

Unit : mm

