TPS62135, TPS621351 High Accuracy 3-V to 17-V 3.5-A Step-Down Converters with DCS-Control™

1 Features

- Output Voltage Accuracy ± 1% (PWM mode)
- Input Voltage Range: 3 V to 17 V
- Quiescent Current 18 µA Typ
- Output Voltage from 0.8 V to 12 V
- Adjustable Soft-Start
- Precise ENABLE input allows
  - User-Defined Undervoltage Lockout
  - Exact Sequencing
- 100% Duty Cycle Mode
- Automatic Efficiency Enhancement AEE™
- DCS-Control™ Topology
- Available with Active Output Discharge
- Optional HICCUP Overcurrent Protection
- Power Good Output
- Available in 3-mm x 2-mm VQFN Package

2 Applications

- Standard 12-V Rail Supplies
- POL for Connected Standby Requirements
- POL Supply from Single or Multiple Li-Ion Battery
- Gaming Consoles, SSD Drives
- Mobile and Embedded Computers

3 Description

The TPS62135 and TPS621351 are high efficiency and easy to use synchronous step-down DC-DC converters, based on the DCS-Control™ Topology. The devices wide input voltage range of 3-V to 17-V makes it suitable for multi-cell Li-Ion as well as 12-V intermediate supply rails. The devices provide 3.5-A continuous output current. The TPS62135 automatically enters Power Save Mode at light loads to maintain high efficiency across the whole load range. With that, the device is well suited for applications that require connected standby performance, like ultra low power computers. With the MODE pin set to low, the switching frequency of the device is adapted automatically based on the input and output voltage. This technique is called Automatic Efficiency Enhancement (AEE™) and maintains high conversion efficiency over the whole operation range. It provides a 1% output voltage accuracy in PWM mode and therefore enables the design of a power supply with high output voltage accuracy.

The device has a typical quiescent current of 18 µA. In shutdown mode the current is typically 1 µA and the output is actively discharged for TPS62135 while the output voltage discharge feature is disabled in TPS621351.

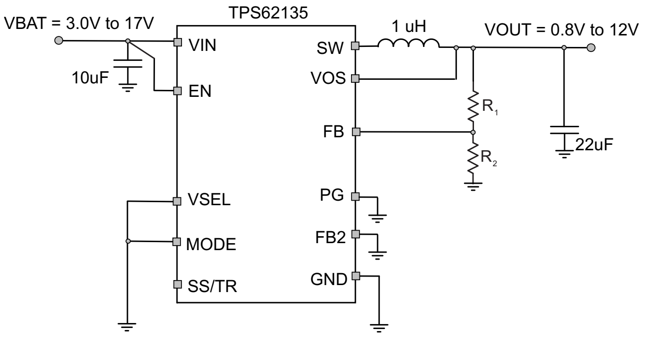
The TPS62135 is available as an adjustable version, packaged in a 3-mm x 2-mm VQFN package.

Device Information(1)

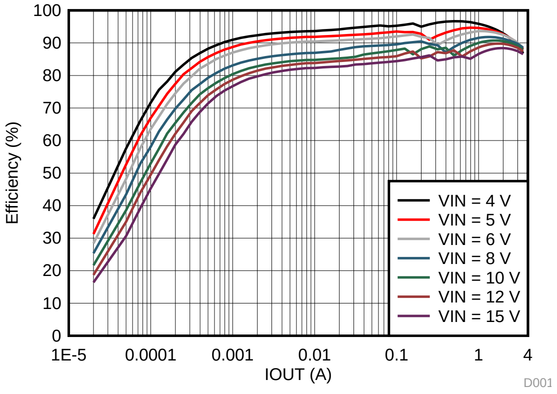
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS62135	VQFN	3.00 mm x 2.00 mm
TPS621351	VQFN	3.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Efficiency vs Output Current for Vo = 3.3 V



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4 Revision History

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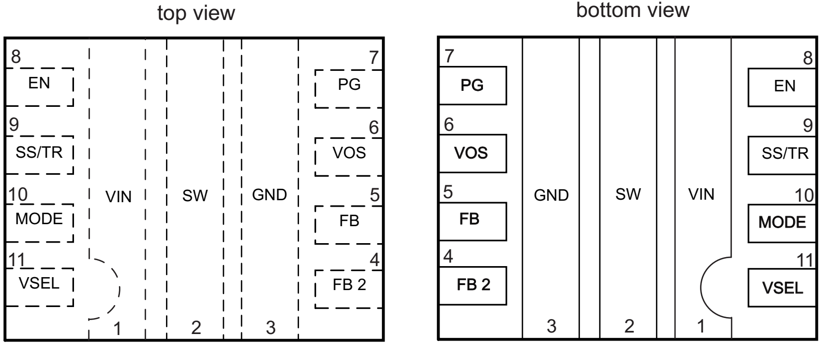
• Changed from Product Preview to Production Data	1

5 Device Comparison Table

DEVICE NUMBER	FEATURES	OUTPUT VOLTAGE	MARKING
TPS62135RGX	output voltage discharge voltage selection input / output VSEL/FB2 nominal switching frequency = 2.5 MHz HICCUP current limit	adjustable	62135
TPS621351RGX	voltage selection input / output VSEL/FB2 nominal switching frequency = 2.5 MHz	adjustable	621351

6 Pin Configuration and Functions

RGX Package
11-Pin VQFN



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
EN	8	I	This is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB	5	I	Voltage feedback input, connect resistive output voltage divider to this pin.
FB2	4	O	Open drain of an internal switch to GND. Allows to turn on a resistor in parallel to the feedback resistor R2 and increase the output voltage with VSEL = high.
GND	3		Ground pin.
MODE	10	I	The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected.
PG	7	O	Open drain power good output.
SS/TR	9	I	Soft-Start / Tracking pin. An external capacitor connected from this pin to GND defines the rise time for the internal reference voltage. The pin can also be used as an input for tracking and sequencing - see *Detailed Description* section in this document.
SW	2		This is the switch pin of the converter and is connected to the internal Power MOSFETs.
VIN	1		Power supply input. Make sure the input capacitor is connected as close as possible between pin VIN and GND.
VOS	6	I	Output voltage sense pin. Connect directly to the positive pin of the output capacitor.
VSEL	11	I	Voltage scaling control input. Turns on an internal switch from FB2 to GND when this pin is set high.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage range(2)	VIN	-0.3	20	V
	SW, VOS	-0.3	V_{IN}+0.3	V
	SW (transient)		23	V
	EN, MODE, VSEL, PG, FB, FB2, SS/TR	-0.3	V_{IN}+0.3	V
Operating junction temperature, T_J		-40	150	°C
Storage temperature range, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model - (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charge Device Model - (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply voltage range	3		17	V
VOUT	Output voltage range	0.8		12	V
L	Effective inductance	0.6	1	2.9	µH
C_O	Effective output capacitance(1)	6	22	200(2)	µF
C_I	Effective input capacitance(1)(3)	3	10		µF
T_J	Operating junction temperature	-40		+125	°C

(1) Due to the dc bias effect of ceramic capacitors, the effective capacitance is lower then the nominal value when a voltage is applied. This is why the capacitance is specified to allow the selection of the smallest capacitor required with the dc bias effect for this type of capacitor in mind. The nominal value given matches a typical capacitor to be chosen to meet the minimum capacitance required.
(2) This is for capacitors directly at the output of the TPS62135x. More capacitance is allowed if there is a series resistance associated to the capacitors. See also the systems examples *Powering Multiple Loads* for applications where many distributed capacitors are connected to the output.
(3) Larger values may be required if the source impedance can not support the transient requirements of the load.

7.4 Thermal Information

THERMAL METRIC[1]		TPS62135, TPS621351 RGX (VQFN) 11 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	2.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report. Thermal data is taken according JEDEC 51-5 on a 4-layer pcb with 6 thermal vias.

7.5 Electrical Characteristics

over operating junction temperature (T_J= -40 °C to +125 °C) and V_{IN}= 3 V to 17 V. Typical values at V_{IN} = 12 V and T_A= 25 °C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating Quiescent Current	EN = high, I_{OUT}= 0 mA, Device not switching, T_J= 85 °C			35	µA
I_Q	Operating Quiescent Current	EN = high, I_{OUT}= 0 mA, Device not switching		18	46	µA
I_{SD}	Shutdown Current	EN = 0 V, Nominal value at T_J= 25 °C, Max value at T_J= 85 °C		1	8	µA
V_{UVLO}	Undervoltage Lockout Threshold	Rising Input Voltage	2.8	2.9	3.0	V
		Falling Input Voltage	2.5	2.6	2.7	V
T_{SD}	Thermal Shutdown Temperature	Rising Junction Temperature		160		°C
	Thermal Shutdown Hysteresis			20		
CONTROL (EN, SS/TR, PG, MODE, VSEL)						
V_{IH}	High Level Input Voltage for VSEL, MODE pin		0.9			V
V_{IL}	Low Level Input Voltage for VSEL, MODE pin				0.3	V
V_{IH}	Input Threshold Voltage for EN pin; rising edge		0.77	0.8	0.83	V
V_{IL}	Input Threshold Voltage for EN pin; falling edge		0.67	0.7	0.73	V
I_{LKG_EN}	Input Leakage Current for EN, VSEL, MODE	V_{IH} = VIN or V_{IL}= GND			100	nA
V_{TH_PG}	Power Good Threshold Voltage; dc level	Rising (%V_{OUT})	93%	96%	98%	
	Hysteresis	Falling (%V_{OUT})	3%		4.5%	
V_{OL_PG}	Power Good Output Low Voltage	I_{PG} = -2 mA		0.07	0.3	V
I_{LKG_PG}	Input Leakage Current (PG)	V_{PG} = 5 V			100	nA
$I_{SS/TR}$	SS/TR pin source current			2.5		µA
	$I_{SS/TR}$ tolerance	T_J= -40 °C to +125 °C		±0.2		µA
	Tracking gain	V_{FB} / $V_{SS/TR}$		1		
	Tracking offset	feedback voltage with $V_{SS/TR}$ = 0 V		11		mV

Electrical Characteristics (continued)

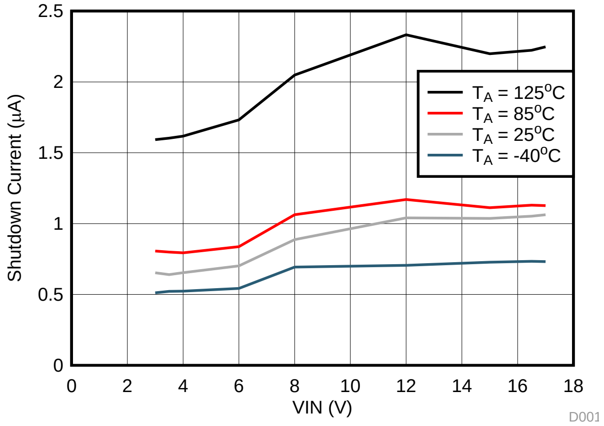
over operating junction temperature (T_J= -40 °C to +125 °C) and V_{IN}= 3 V to 17 V. Typical values at V_{IN} = 12 V and T_A= 25 °C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(ON)}$	High-Side MOSFET ON-Resistance	V_{IN} ≥ 4 V			100	180	mΩ
	Low-Side MOSFET ON-Resistance	V_{IN} ≥ 4 V			39	67	mΩ
I_{LIMH}	High-Side MOSFET Current Limit	dc value[1]		4.4	5.2	6.5	A
I_{LIML}	Low-Side MOSFET Current Limit	dc value[1]		4.4	5.2	6.5	A
I_{LIMNEG}	Negative current limit; average value	dc value			1.5		A
OUTPUT							
V_{FB}	Feedback Voltage				0.7		V
I_{LKG_FB}	Input Leakage Current (FB)	V_{FB}= 0.7 V			1	70	nA
V_{FB}	Feedback Voltage Accuracy[2]	V_{IN} ≥ V_{OUT} +1 V	PWM mode	-1%		1%	
		V_{IN} ≥ V_{OUT} +1 V; V_{OUT} ≥ 1.5 V	PFM mode; Co,eff ≥ 47 µF, L = 1 µH	-1%		2%	
		1 V ≤ V_{OUT} < 1.5 V	PFM mode; Co,eff ≥ 4 7 µF, L = 1 µH	-1%		2.5%	
		V_{OUT} < 1 V	PFM mode; Co,eff ≥ 75 µF, L = 1 µH	-1%		2.5%	
V_{FB}	Feedback Voltage Accuracy with Voltage Tracking	V_{IN} ≥ V_{OUT} +1 V; $V_{SS/TR}$ = 0.35 V	PWM mode	-2%		7.5%	
$R_{DS(ON)}$	FB2 resistance to GND when VSEL= high				10	30	Ω
I_{LKG_FB2}	Input Leakage Current in FB2 when VSEL = low				1	70	nA
	Load Regulation	PWM mode operation			0.05		%/A
	Line Regulation	PWM mode operation, I_{OUT}= 1 A, VIN ≥ Vout + 1 V or VIN ≥ 3.5 V whichever is larger			0.02		%/V
	Output Discharge Resistance	TPS62135 only			100		Ω
t_{delay}	Start-up Delay time	I_O= 0 mA, Time from EN=high to start switching; VIN applied already			200	300	µs
t_{ramp}	Ramp time; SS/TR pin open	I_O= 0 mA, Time from first switching pulse until 95% of nominal output voltage; device not in current limit			150		µs

(1) See also *HICCUP Current Limit And Short Circuit Protection (TPS62135 only)* and *Current Limit And Short Circuit Protection (TPS621351 only)*.

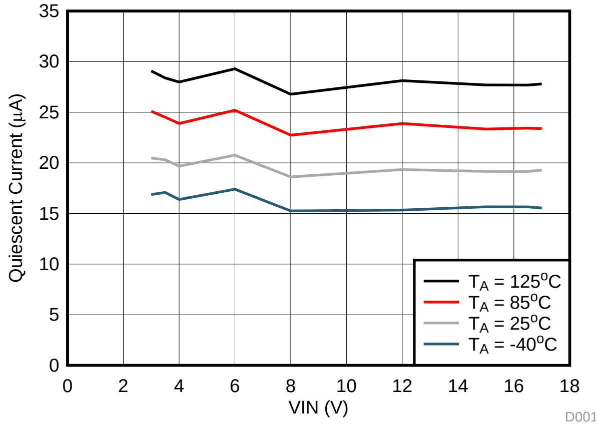
(2) The output voltage accuracy in Power Save Mode can be improved by increasing the output capacitor value, reducing the output voltage ripple (see *Pulse Width Modulation (PWM) Operation*).

7.6 Typical Characteristics



EN = low

Figure 1. Shutdown Current vs Input Voltage



EN = high device not switching

Figure 2. Quiescent Supply Current vs Input Voltage

8 Parameter Measurement Information

8.1 Schematic

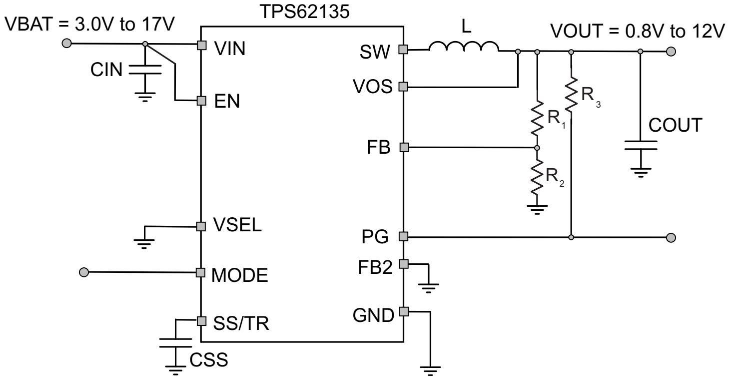


Figure 3. Measurement Setup

Table 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	17 V, 3.5 A Step-Down Converter	TPS62135; Texas Instruments
L	1 µH inductor	XFL4020-102; Coilcraft
CIN	10 µF, 25 V, Ceramic, 0805	TMK212BBJ106MG-T; Taiyo Yuden
COUT	2 x 10 µF, 16 V, Ceramic, 0805; all VOUT except 9 V and 1.2 V	EMK212BBJ106MG-T; Taiyo Yuden
COUT	3 x 10 µF, 16 V, Ceramic, 0805 for VOUT = 1.2 V	EMK212BBJ106MG-T; Taiyo Yuden
COUT	4 x 10 µF, 16 V, Ceramic, 0805 for VOUT = 9 V	EMK212BBJ106MG-T; Taiyo Yuden
CSS	3.3 nF, 10 V, Ceramic, X7R	-
R1	Depending on Vout; see Table 5	Standard 1% metal film
R2	Depending on Vout; see Table 5	Standard 1% metal film
R3	470 kΩ, Chip, 0603, 1/16 W, 1%	Standard 1% metal film

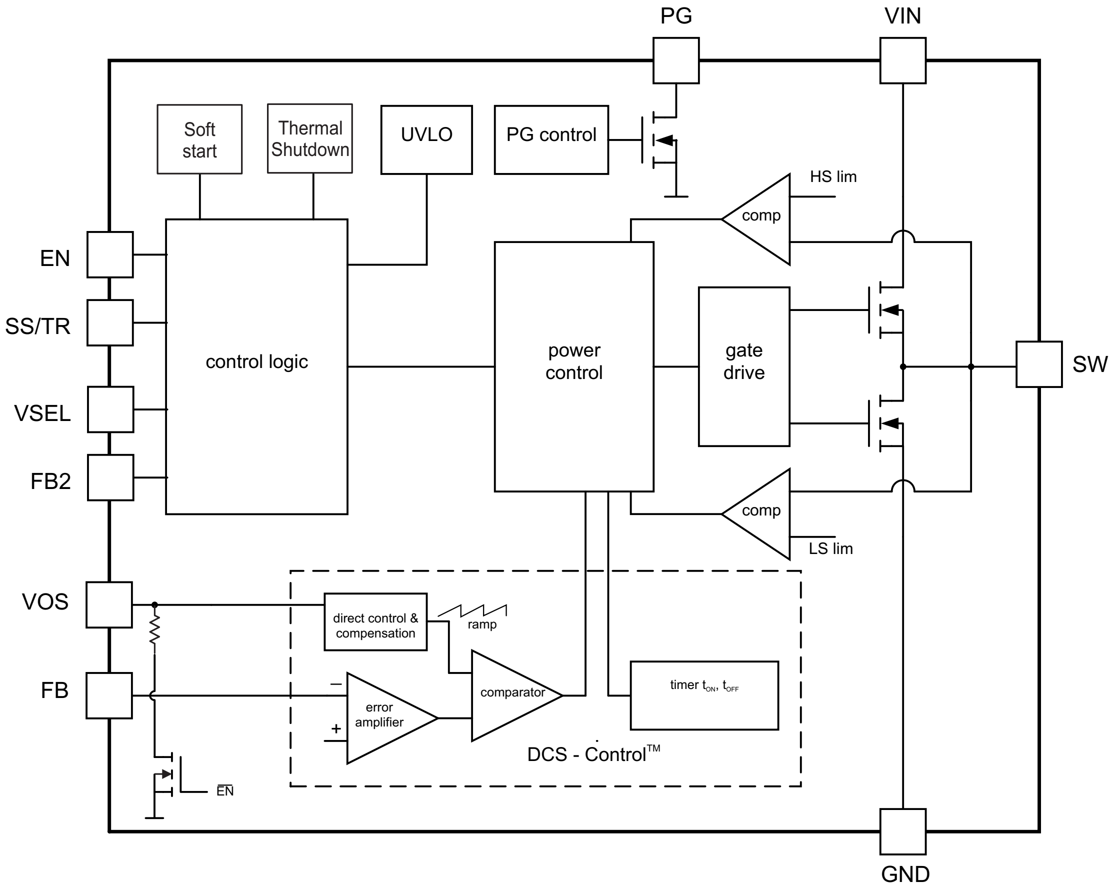
9 Detailed Description

9.1 Overview

The TPS62135 synchronous switched mode power converters are based on DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports PWM (Pulse Width Modulation) mode for medium and heavy load conditions and a Power Save Mode at light loads. During PWM, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.5 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters Power Save Mode to sustain high efficiency down to very light loads. In Power Save Mode the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to Power Save Mode is seamless without effects on the output voltage. An internal current limit supports nominal output currents of up to 3.5 A. The TPS62135x family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

9.2 Functional Block Diagram



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The discharge switch on the VOS pin is only available in the TPS62135.

9.3 Feature Description

9.3.1 Precise Enable

The voltage applied at the Enable pin of the TPS62135x is compared to a fixed threshold of 0.8 V for a rising voltage. This allows to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a power-up delay.

The Precise Enable input allows the use as a user programmable undervoltage lockout by adding a resistor divider to the input of the Enable pin.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The TPS62135x starts operation when the rising threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown, with a shutdown current of typically 1 μA. In this mode, the internal high side and low side MOSFETs are turned off and the entire internal control circuitry is switched off.

9.3.2 Power Good (PG)

The TPS62135x has a built in power good (PG) function to indicate whether the output voltage has reached its target. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor to any voltage up to a voltage level of the input voltage at VIN. It can sink 2 mA of current and maintain its specified logic low level. PG is low when the device is turned off due to EN, UVLO or thermal shutdown, so it can be used to actively discharge Vout. VIN must remain present for the PG pin to stay low.

In case VSEL is used to change the output voltage during operation, PG is not blanked for a change from low output voltage to high output voltage. It therefore will indicate "power bad" if the voltage step is large enough to trigger the power good comparator. The power good threshold in transient operation may slightly different from the dc values given in the electrical specification in case a feed forward capacitor is used on the output voltage divider. Due to the capacitive coupling, power good can go high for a short time after a release of a short circuit on the output.

If the power good output is not used, it is recommended to tie to GND or leave open.

9.3.3 Pin-Selectable Output Voltage (VSEL and FB2)

The output voltage of the TPS62135x is set by the resistor divider from VOUT to FB to GND. The topology requires a voltage divider on FB, so the minimum output voltage is 0.8 V while the feedback voltage on the FB pin is 0.7 V.

VSEL and FB2 can optionally be used to enable a second resistor from FB2 to GND which increases the divider ratio, hence increasing the output voltage. See Typical Application using VSEL and FB2 .

9.3.4 MODE

When MODE is set low, the device operates in PWM or PFM mode depending on the output current. Automatic Efficiency Enhancement (AEE) is enabled for highest efficiency over a wide input voltage, output voltage and output current range. The MODE pin allows to force PWM mode when set high. In forced PWM mode, AEE is disabled. See also *Power Save Mode Operation (PWM/PFM)*.

9.3.5 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the power FETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage trips below the threshold for a falling supply voltage.

9.3.6 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 160°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis amount of typically 20°C, the converter resumes normal operation, beginning with Soft-Start. During a PFM skip pause, the thermal shutdown is not active. See also *Power Save Mode Operation (PWM/PFM)*.

9.4 Device Functional Modes

9.4.1 Pulse Width Modulation (PWM) Operation

TPS62135x has two operating modes: Forced PWM mode discussed in this section and PWM/PFM as discussed in *Power Save Mode Operation (PWM/PFM)*.

With the MODE pin set to high, the TPS62135x operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of 2.5 MHz. The frequency variation in PWM is controlled and depends on VIN, VOUT and the inductance. The on-time in forced PWM mode is given by:

$$TON = \frac{VOUT}{VIN} \times 400[ns] \tag{1}$$

9.4.2 Power Save Mode Operation (PWM/PFM)

When the MODE pin is low, Power Save Mode is allowed. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters Power Save Mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current. For improved transient response, PWM mode is forced for 8 switching cycles if the output voltage is above target due to a load release. The Power Save Mode is entered seamlessly, if the load current decreases and the MODE pin is set low. This ensures a high efficiency in light load operation. The device remains in Power Save Mode as long as the inductor current is discontinuous.

In Power Save Mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of Power Save Mode is seamless in both directions.

The AEE function in TPS62135 and TPS621351 adjust the on-time (TON) in power save mode depending on the input voltage and the output voltage to maintain highest efficiency. The on-time, in steady-state operation, can be estimated as:

$$TON = 100 \times \frac{VIN}{VIN - VOUT}[ns] \tag{2}$$

For very small output voltages, an absolute minimum on-time of about 50 ns is kept to limit switching losses. The operating frequency is thereby reduced from its nominal value, which keeps efficiency high. Using TON, the typical peak inductor current in Power Save Mode is approximated by:

$$ILPSM_{(peak)} = \frac{(VIN - VOUT)}{L} \times TON \tag{3}$$

There is a minimum off-time which limits the duty cycle of the TPS62135x. When V_{IN} decreases to typically 15% above VOUT, the TPS62135x does not enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

The output voltage ripple in power save mode is given by Equation 4:

$$\Delta V = \frac{L \times VIN^2}{200 \times C}\left(\frac{1}{VIN - VOUT} + \frac{1}{VOUT}\right) \tag{4}$$

9.4.3 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by D = VOUT/VIN and increases as the input voltage comes close to the output voltage. The minimum off-time is about 80 ns. When the minimum off-time is reached, TPS62135x scales down its switching frequency while it approaches 100% mode. In 100% mode it keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences, for example for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, can be calculated as:

$$VIN_{(min)} = VOUT + IOUT\left(R_{DS(on)} + R_L\right) \tag{5}$$

Device Functional Modes (continued)

where:

IOUT is the output current,

$R_{DS(on)}$ is the on-state resistance of the high-side FET and

R_L is the DC resistance of the inductor used.

9.4.4 HICCUP Current Limit And Short Circuit Protection (TPS62135 only)

The TPS62135 is protected against overload and short circuit events. If the inductor current exceeds the current limit I(LIMF), the high side switch is turned off and the low side switch is turned on to ramp down the inductor current. Once the switch current limit is triggered for 512 switching cycles, the device stops switching. After a typical delay of 800 µs, the device begins a new Soft-Start cycle. This is called HICCUP short circuit protection. TPS62135 repeats this mode until the short circuit condition disappears.

Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD} \tag{6}$$

where:

I_{LIMF} is the static current limit as specified in the electrical characteristics

L is the effective inductance at the peak current

V_L is the voltage across the inductor (V_{IN} - V_{OUT}) and

t_{PD} is the internal propagation delay of typically 50 ns.

The current limit can exceed static values, especially if the input voltage is high and very small inductances are used. The dynamic high side switch peak current can be calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{VIN - VOUT}{L} \times 50ns \tag{7}$$

9.4.5 Current Limit And Short Circuit Protection (TPS621351 only)

The TPS621351 is protected by a current limit the same as the TPS62135 but does not turn off after a certain time. This allows it to provide the maximum current, for example, charging a large output capacitance without the need to increase the Soft-Start time. Equation 6 and Equation 7 also apply.

9.4.6 Soft-Start / Tracking (SS/TR)

The internal Soft-Start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high to start operation, the device starts switching after a delay of about 200 µs then the internal reference and hence VOUT rises with a slope controlled by an external capacitor connected to the SS/TR pin.

Leaving SS/TR pin un-connected provides fastest startup behavior with 150 µs typically.

If the device is set to shutdown (EN = GND), undervoltage lockout or thermal shutdown, an internal resistor pulls the SS/TR pin down to ensure a proper low level. Returning from those states causes a new startup sequence as set by the SS/TR connection.

A voltage supplied to SS/TR can be used to track a master voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current. The SS/TR pin of several devices must not be connected with each other.

Device Functional Modes (continued)

9.4.7 Output Discharge Function (TPS62135 only)

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active once TPS62135 has been enabled at least once since the supply voltage was applied. The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled, in thermal shutdown or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active typically is 2 V. Output discharge is not activated during a HICCUP current limit event.

9.4.8 Starting into a Pre-Biased Load (TPS621351 only)

The TPS621351 is capable of starting into a pre-biased output. The device only starts switching when the internal Soft-Start ramp is equal or higher than the feedback voltage. If the voltage at the feedback pin is biased to a higher voltage than the nominal value, the TPS621351 does not start switching unless the voltage at the feedback pin drops to the target.

This functionality actually also applies to TPS62135 but the discharge function in TPS62135 keeps the voltage close to 0 V, so starting into a pre-biased output does not apply.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Programming the Output Voltage

The output voltage of the TPS62135x is adjustable. It can be programmed for output voltages from 0.8 V to 12 V, using a resistor divider from VOUT to GND. The voltage at the FB pin is regulated to 700 mV. The value of the output voltage is set by the selection of the resistor divider from Equation 8. It is recommended to choose resistor values which allow a current of at least 2 uA, meaning the value of R2 should not exceed 400 kΩ. Lower resistor values are recommended for highest accuracy and most robust design.

$$R_1 = R_2\left(\frac{VOUT}{VFB} - 1\right) \tag{8}$$

10.1.2 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the device´s control loop. The TPS62135x is optimized to work within a range of external components. The LC output filters inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see *Output Filter and Loop Stability*). Table 2 can be used to simplify the output filter component selection.

Table 2. Recommended LC Output Filter Combinations[1]

	4.7 µF	10 µF	22 µF	47 µF	100 µF	200 µF	≥400 µF
0.68 µH		√	√	√			
1 µH		√	√[2]	√	√	√	√[3]
1.5 µH		√	√	√	√	√	√[3]
2.2 µH		√	√	√	√	√	√[3]
3.3 µH							

(1) The values in the table are nominal values.
(2) This LC combination is the standard value and recommended for most applications.
(3) Output capacitance needs to have a ESR of ≥ 10 mΩ for stable operation, see also *Powering Multiple Loads*.

10.1.3 Inductor Selection

The TPS62135x is designed for a nominal 1-µH inductor. Larger values can be used to achieve a lower inductor current ripple but they may have a negative impact on efficiency and transient response. Smaller values than 1µH will cause a larger inductor current ripple which causes larger negative inductor current in forced PWM mode at low or no output current. Therefore they are not recommended at large voltages across the inductor as it is the case for high input voltages and low output voltages. With low output current in forced PWM mode this causes a larger negative inductor current peak which may exceed the negative current limit. More detailed information on further LC combinations can be found in SLVA463.

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PFM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). Equation 9 calculates the maximum inductor current.

$$I_{L(\max)} = I_{OUT(\max)} + \frac{\Delta I_{L(\max)}}{2} \tag{9}$$

$$\Delta I_{L(\max)} = \frac{VIN_{(\max)}}{L_{(\min)}} \times 100ns \tag{10}$$

where:

I_L(max) is the maximum inductor current
ΔI_L is the Peak to Peak Inductor Ripple Current
L(min) is the minimum effective inductor value.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS62135x and are recommended for use:

Table 3. List of Inductors

TYPE	INDUCTANCE [µH]	CURRENT [A](1)	DIMENSIONS [LxBxH] mm	MANUFACTURER
XFL4020-102ME	1.0 µH, ±20%	5.4	4 x 4 x 2.1	Coilcraft
XAL4020-102ME	1.0 µH, ±20%	8.7	4 x 4 x 2.1	Coilcraft
XAL4020-152ME	1.5 µH, ±20%	7.1	4 x 4 x 2.1	Coilcraft
XFL4030-102ME	1.0 µH, ±20%	4.1	4 x 4 x 3.1	Coilcraft
1277AS-H-1R0M (DFE322512C)	1.0 µH, ±20%	3.1(2)	3.2 x 2.5 x 1.2	Murata

(1) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.
(2) For smallest size solutions that in average do not require the full output current TPS62135x can provide.

The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2}\Delta I_L \tag{11}$$

10.1.4 Capacitor Selection

10.1.4.1 Output Capacitor

The recommended value for the output capacitor is 22 µF. The architecture of the TPS62135x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using a higher value has advantages like smaller voltage ripple and a tighter DC output accuracy in Power Save Mode (see SLVA463).

In Power Save Mode, the output voltage ripple depends on the output capacitance, its ESR, ESL and the peak inductor current. Using ceramic capacitors provides small ESR, ESL and low ripple. The output capacitor needs to be as close as possible to the device.

For large output voltages the dc bias effect of ceramic capacitors is large and the effective capacitance has to be observed.

10.1.4.2 Input Capacitor

For most applications, 10 µF nominal is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor (MLCC) is recommended for best filtering and should be placed between VIN and GND as close as possible to those pins.

Table 4. List of Capacitors(1)

TYPE	NOMINAL CAPACITANCE [µF]	VOLTAGE RATING [V]	SIZE	MANUFACTURER
TMK212BBJ106MG-T	10	25	0805	Taiyo Yuden
EMK212BBJ226MG-T	22	16	0805	Taiyo Yuden

(1) Lower of I_{RMS} at 40°C rise or I_{SAT} at 30% drop.

10.1.4.3 Soft-Start Capacitor

A capacitor connected between SS/TR pin and GND allows a user programmable start-up slope of the output voltage. A constant current source provides typically 2.5 µA to charge the external capacitance. The capacitor required for a given Soft-Start ramp time is given by:

$$C_{SS} = t_{SS} \times \frac{2.5\mu A}{0.7V} \; [F] \tag{12}$$

where:

C_{SS} is the capacitance required at the SS/TR pin and
t_{SS} is the desired Soft-Start ramp time

The fastest achievable typical ramp time is 150 µs even if the external C_{ss} capacitance is lower than 680 pF or the pin is open.

10.1.5 Tracking Function

If a tracking function is desired, the SS/TR pin can be used for this purpose by connecting it to an external tracking voltage. The output voltage tracks that voltage with the typical gain and offset as specified in the electrical characteristics.

When the SS/TR pin voltage is above 0.7 V, the internal voltage is clamped and the device goes to normal regulation. This works for rising and falling tracking voltages with the same behavior, as long as the input voltage is inside the recommended operating conditions. For decreasing SS/TR pin voltage in PFM mode, the device does not sink current from the output. The resulting decrease of the output voltage may therefore be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is V_{IN} + 0.3 V. The SS/TR pin is internally connected with a resistor to GND when EN = 0.

If the input voltage drops below undervoltage lockout, the output voltage will go to zero, independent of the tracking voltage. Figure 4 shows how to connect devices to get ratiometric and simultaneous sequencing by using the tracking function. See also *Voltage Tracking* in the systems examples. SS/TR is internally clamped to approximately 3 V.

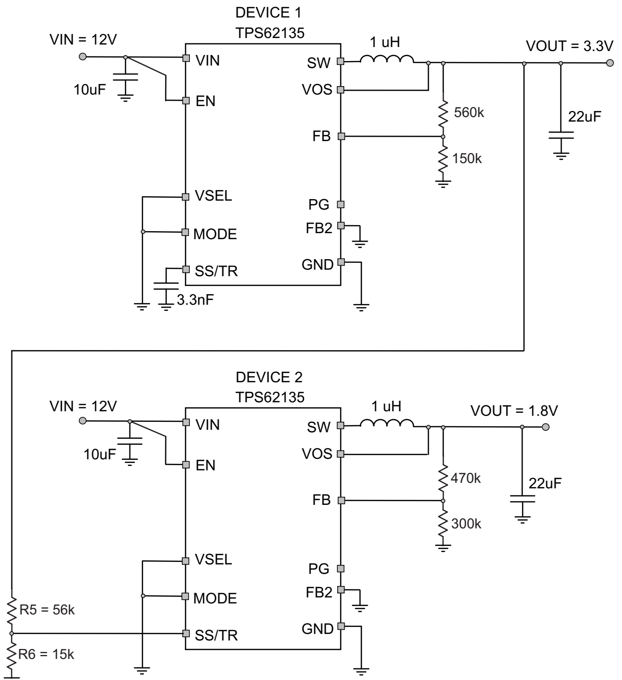

Figure 4. Schematic for Ratiometric and Simultaneous Startup

The resistive divider of R5 and R6 can be used to change the ramp rate of VOUT2 to be faster, slower or the same as VOUT1.

A sequential startup is achieved by connecting the PG pin of VOUT of DEVICE 1 to the EN pin of DEVICE2. PG requires a pull-up resistor. Ratiometric start up sequence happens if both supplies are sharing the same Soft-Start capacitor. Equation 12 gives the Soft-Start time, though the SS/TR current has to be doubled. Details about these and other tracking and sequencing circuits are found in SLVA470.

Note: If the voltage at the FB pin is below its typical value of 0.7 V, the output voltage accuracy may have a wider tolerance than specified. The current of 2.5 µA out of the SS/TR pin also has an influence on the tracking function, especially for high resistive external voltage dividers on the SS/TR pin.

10.1.6 Output Filter and Loop Stability

The devices of the TPS6213X family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency to be calculated with Equation 13:

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \tag{13}$$

Proven nominal values for inductance and ceramic capacitance are given in Table 2 and are recommended for use. Different values may work, but care has to be taken on the loop stability which is affected. More information including a detailed LC stability matrix can be found in SLVA463.

The TPS62135x devices include an internal 15 pF feedforward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per equation Equation 14 and Equation 15:

$$f_{zero} = \frac{1}{2\pi \times R_1 \times 15\,pF} \tag{14}$$

$$f_{pole} = \frac{1}{2\pi \times 15\,pF}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{15}$$

Though the TPS6213x devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in Power Save mode and/or improved transient response. An external feedforward capacitor can also be added. A more detailed discussion on the optimization for stability versus transient response can be found in SLVA289 and SLVA466.

10.2 Typical Applications

10.2.1 Typical Application with Adjustable Output Voltage

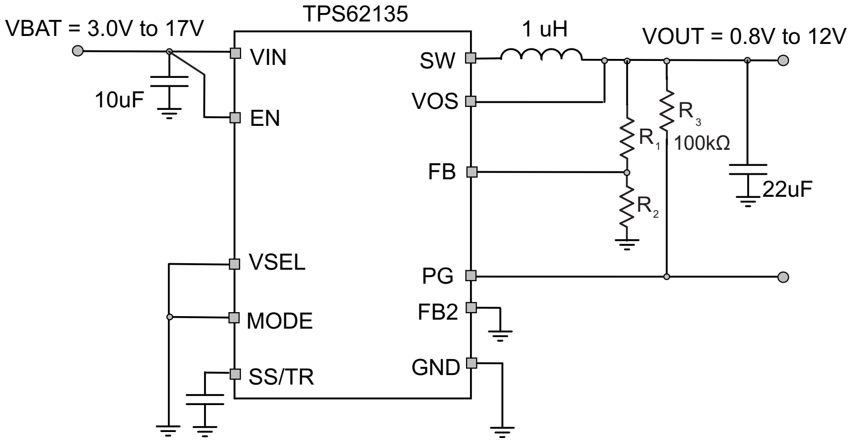

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Figure 5. Typical Application

Typical Applications (continued)

10.2.1.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions. See Table 1 for the Bill of Materials used to generate the application curves.

10.2.1.2 Detailed Design Procedure

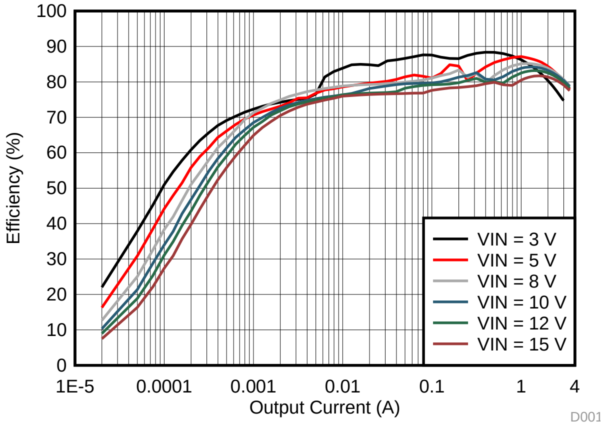
$$R_1 = R_2\left(\frac{VOUT}{VFB} - 1\right) \tag{16}$$

With VFB = 0.7 V:

Table 5. Setting the Output Voltage

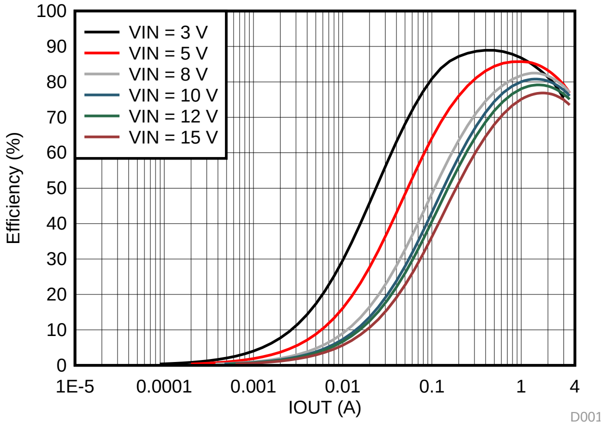
NOMINAL OUTPUT VOLTAGE	R1	R2	EXACT OUTPUT VOLTAGE
0.8 V	51 kΩ	360 kΩ	0.799 V
1.2 V	130 kΩ	180 kΩ	1.206 V
1.5 V	150 kΩ	130 kΩ	1.508 V
1.8 V	470 kΩ	300 kΩ	1.797 V
2.5 V	620 kΩ	240 kΩ	2.508 V
3.3 V	560 kΩ	150 kΩ	3.313 V
5 V	510 kΩ	82 kΩ	5.054 V
9 V	510 kΩ	43 kΩ	9.002 V
12 V	1000 kΩ	62 kΩ	11.99 V

10.2.1.3 Application Curves



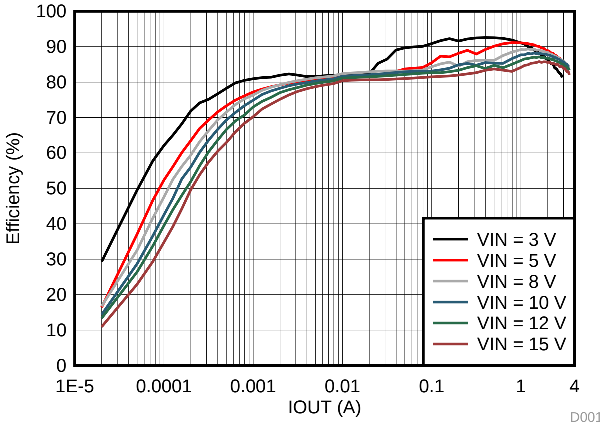
Vout = 1.2 V PFM T_A= 25 °C

Figure 6. Efficiency vs Output Current



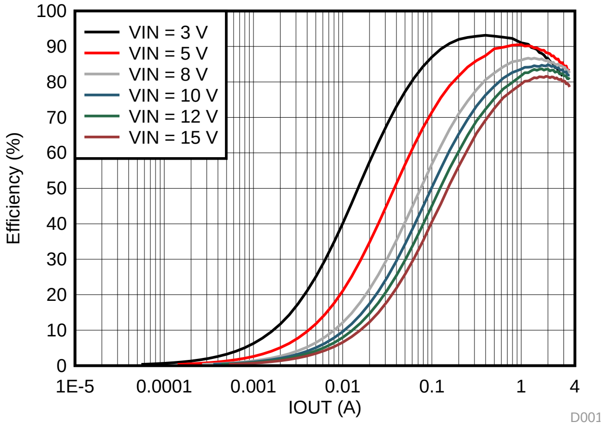
Vout = 1.2 V PWM T_A= 25 °C

Figure 7. Efficiency vs Output Current



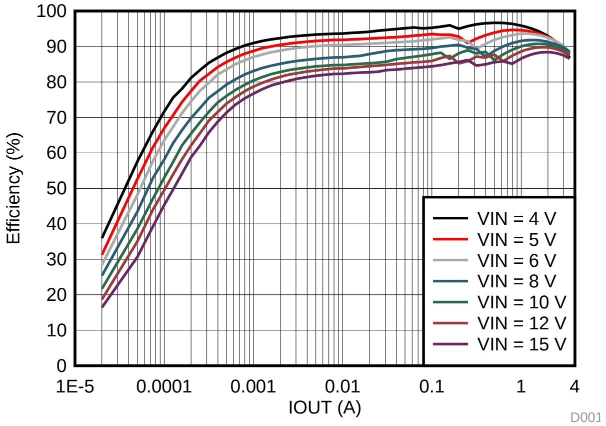
Vout = 1.8 V PFM T_A= 25 °C

Figure 8. Efficiency vs Output Current



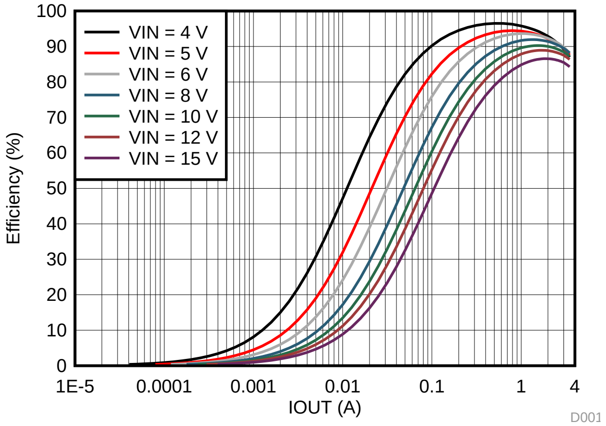
Vout = 1.8 V PWM T_A= 25 °C

Figure 9. Efficiency vs Output Current



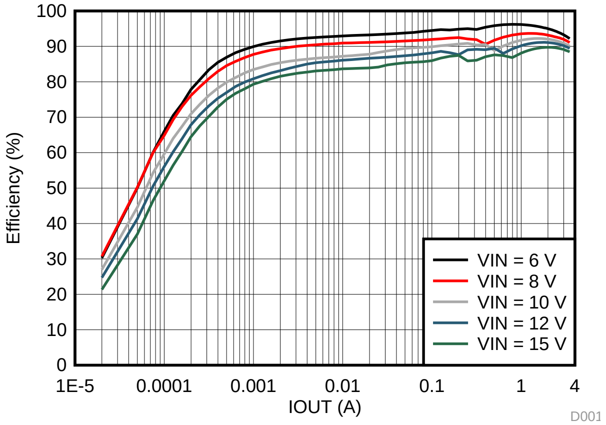
Vout = 3.3 V PFM T_A= 25 °C

Figure 10. Efficiency vs Output Current



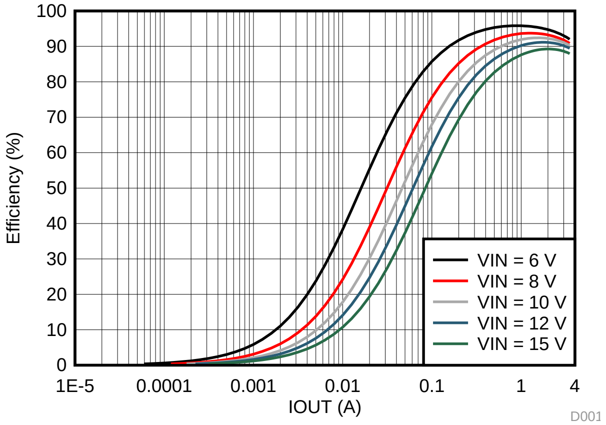
Vout = 3.3 V PWM T_A= 25 °C

Figure 11. Efficiency vs Output Current



Vout = 5 V PFM T_A= 25 °C

Figure 12. Efficiency vs Output Current



Vout = 5 V PWM T_A= 25 °C

Figure 13. Efficiency vs Output Current

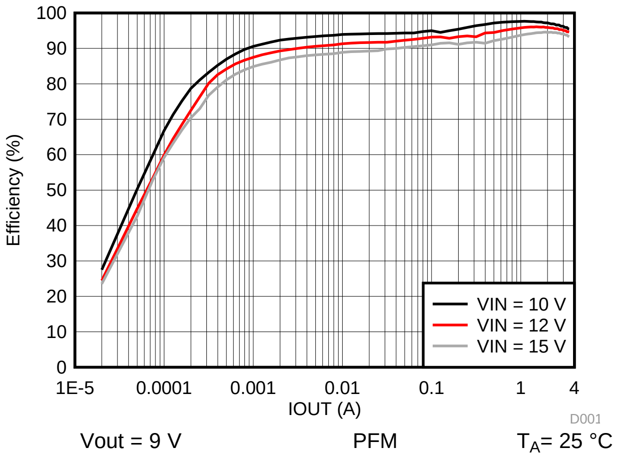


Figure 14. Efficiency vs Output Current

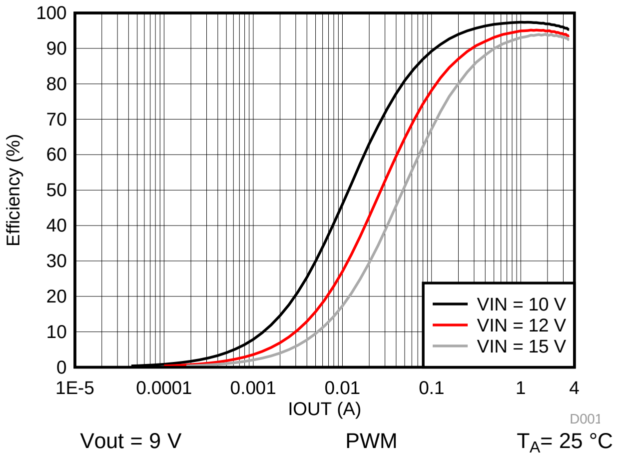


Figure 15. Efficiency vs Output Current

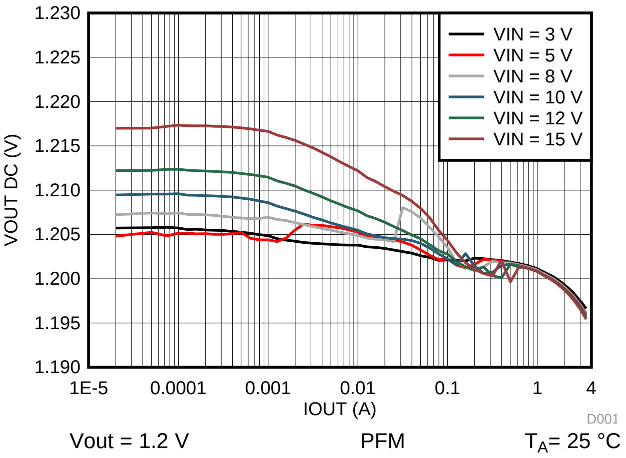


Figure 16. Output Voltage vs Output Current

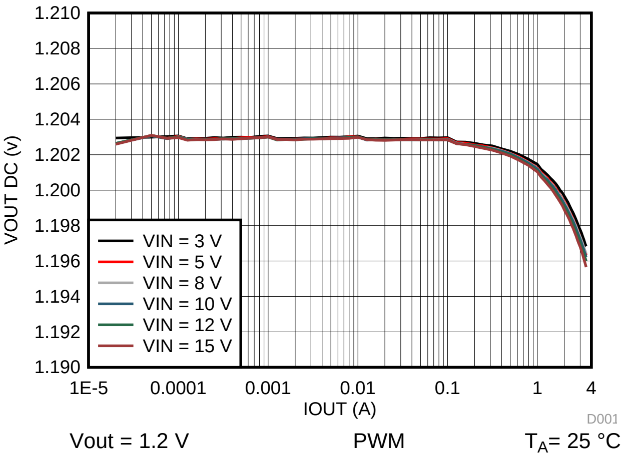


Figure 17. Output Voltage vs Output Current

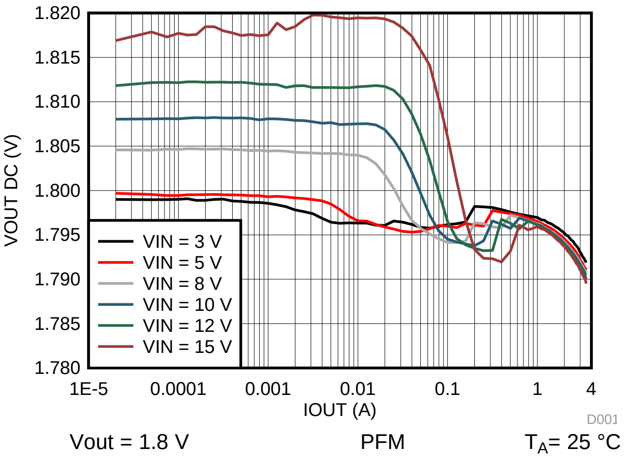


Figure 18. Output Voltage vs Output Current

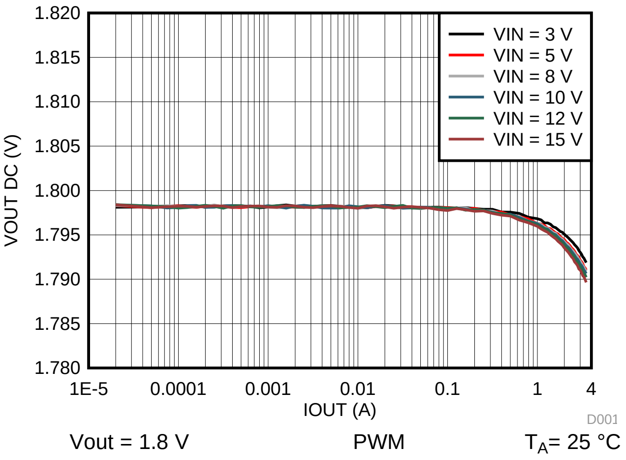


Figure 19. Output Voltage vs Output Current

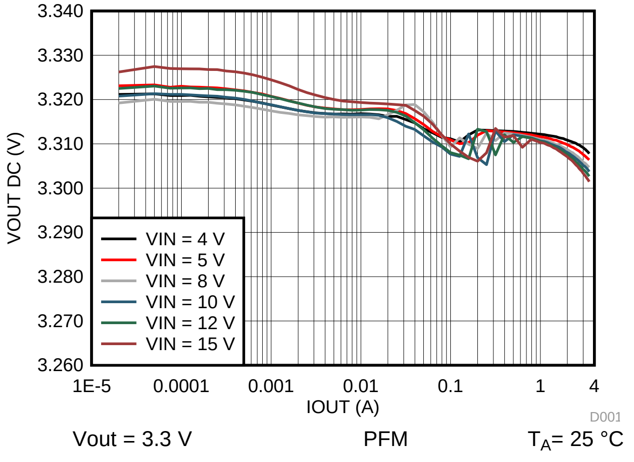


Figure 20. Output Voltage vs Output Current

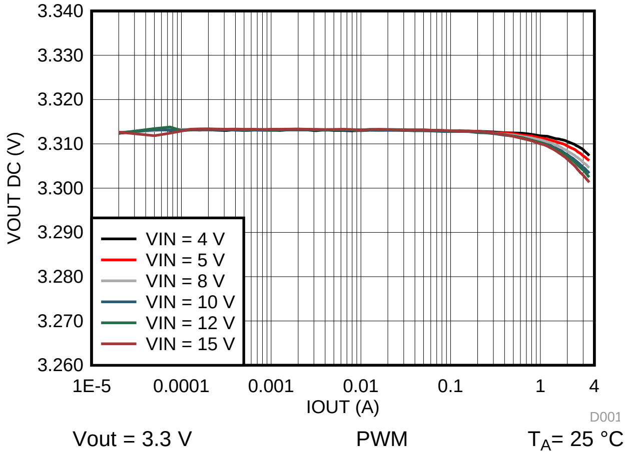


Figure 21. Output Voltage vs Output Current

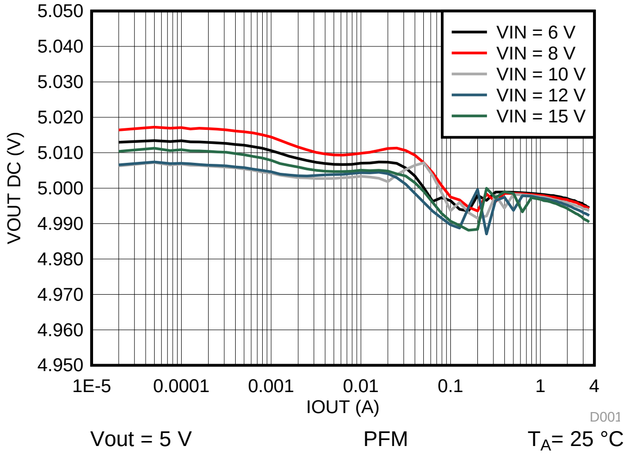


Figure 22. Output Voltage vs Output Current

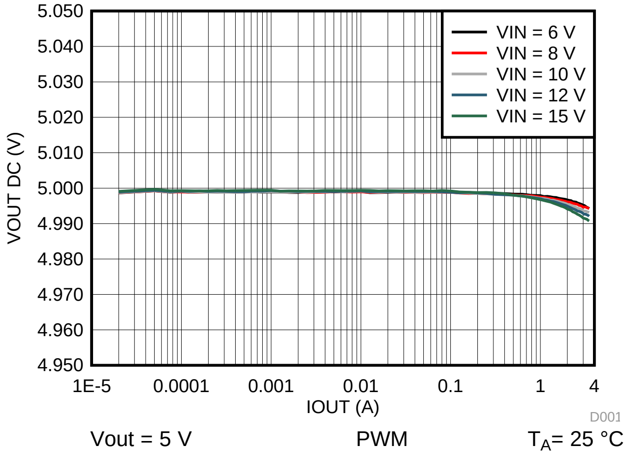


Figure 23. Output Voltage vs Output Current

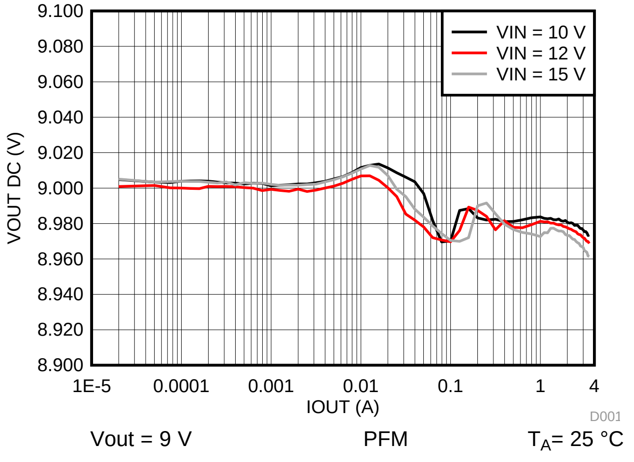


Figure 24. Output Voltage vs Output Current

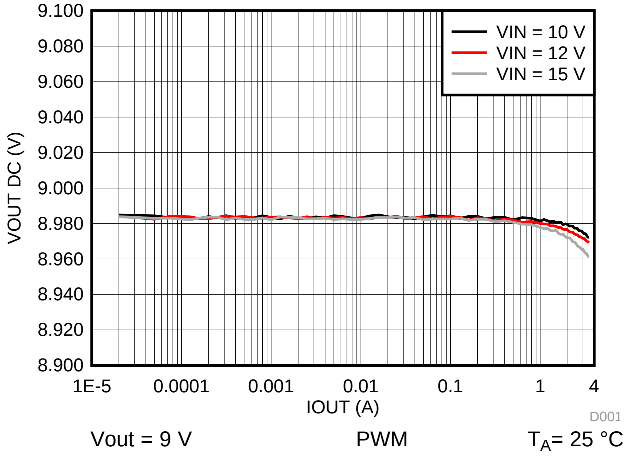
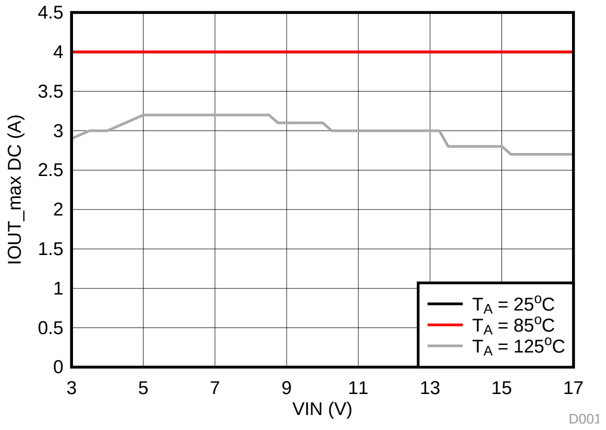


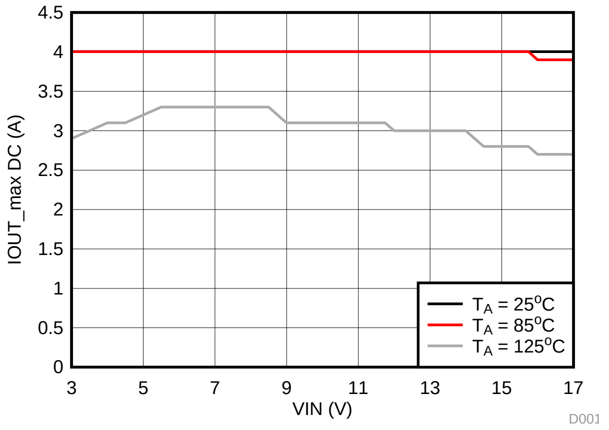
Figure 25. Output Voltage vs Output Current



Vout = 1.2 V PWM measurement taken until 4 A

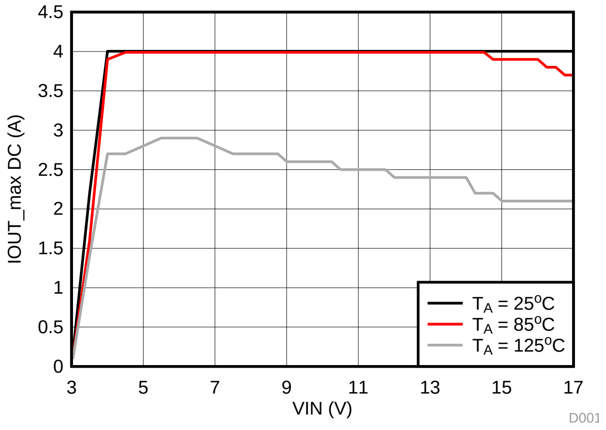
Curves for T_A= 25 °C and T_A= 85 °C overlap

Figure 26. Maximum Output Current vs Input Voltage



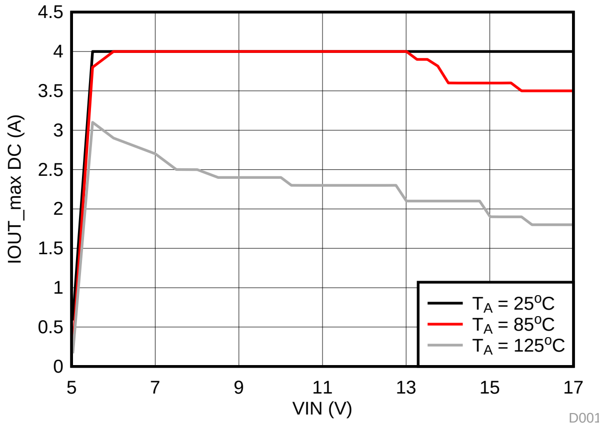
Vout = 1.8 V PWM measurement taken until 4 A

Figure 27. Maximum Output Current vs Input Voltage



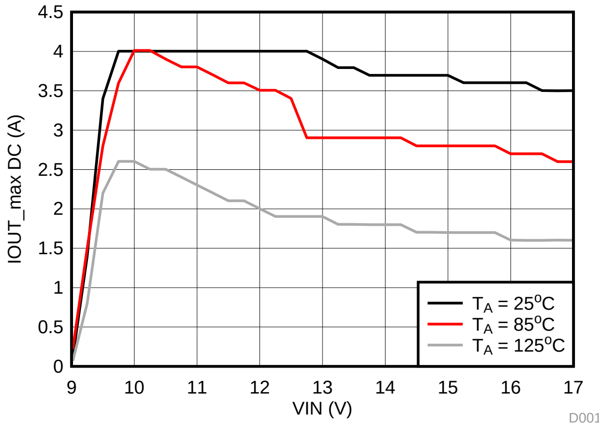
Vout = 3.3 V PWM measurement taken until 4 A

Figure 28. Maximum Output Current vs Input Voltage



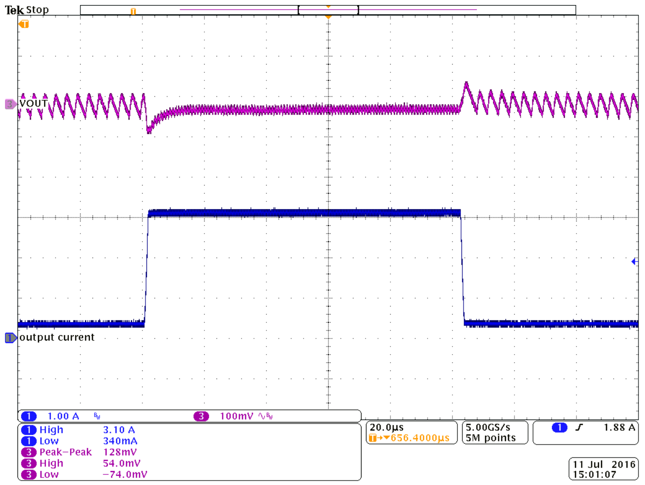
Vout = 5 V PWM measurement taken until 4 A

Figure 29. Maximum Output Current vs Input Voltage



Vout = 9 V PWM measurement taken until 4 A

Figure 30. Maximum Output Current vs Input Voltage

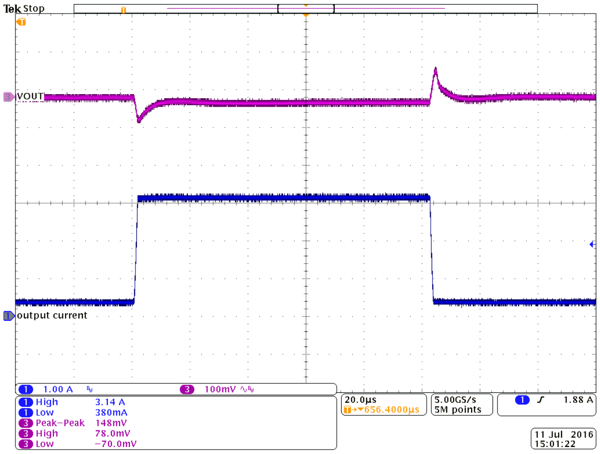


1 High 3.10 A
1 Low 340mA
3 Peak–Peak 128mV
3 High 54.0mV
3 Low −74.0mV

Vin = 12 V; PFM Io = 350 mA to 3.1 A;

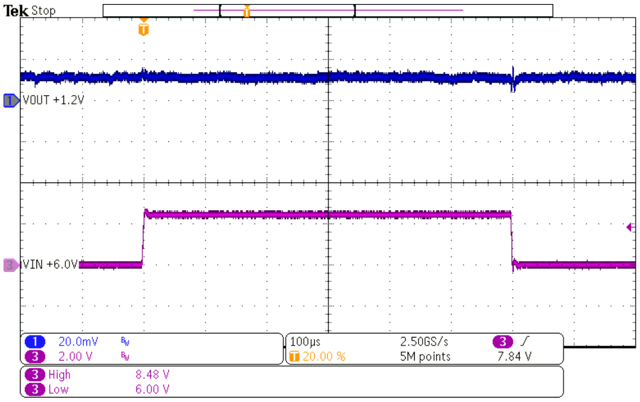
Vout = 1.2 V; T_A= 25 °C

Figure 31. Load Transient Response



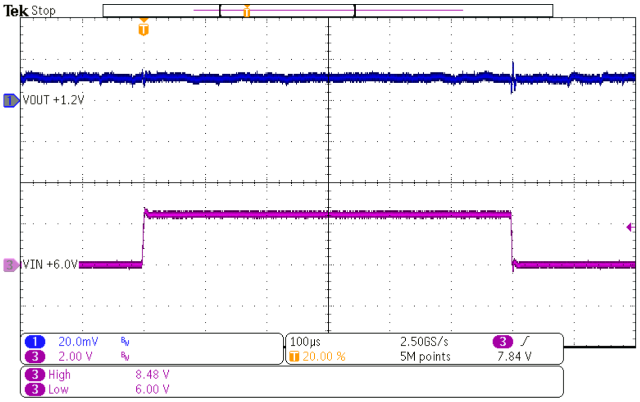
Vin = 12 V; PWM Io = 350 mA to 3.1 A
Vout = 1.2 V T_A= 25 °C

Figure 32. Load Transient Response



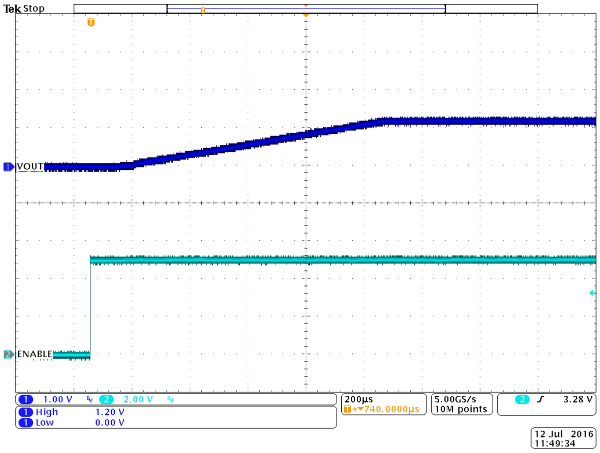
Vin = 6 V to 8.4 V; PFM Io = 1 A
Vout = 1.2 V T_A= 25 °C

Figure 33. Line Transient Response



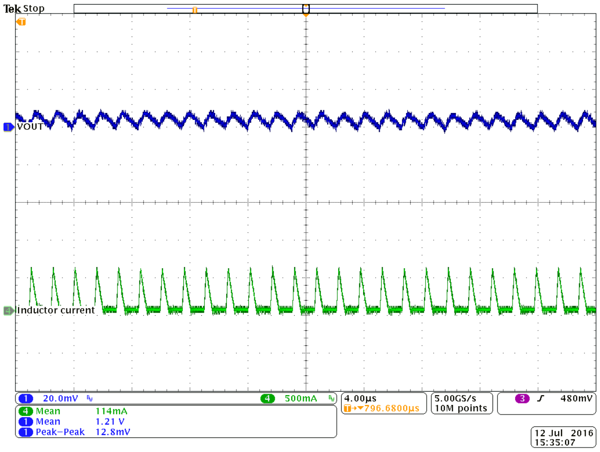
Vin = 6 V to 8.4 V; PWM Io = 1 A
Vout = 1.2 V T_A= 25 °C

Figure 34. Line Transient Response



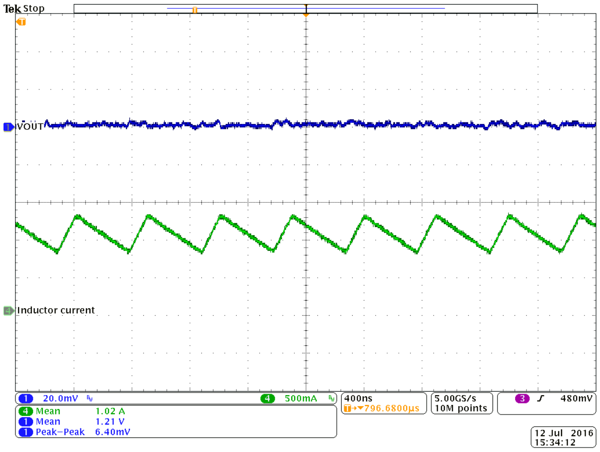
Vin = 5 V; PWM Rload = 1 kΩ
Vout = 1.2 V T_A= 25 °C

Figure 35. Start-Up Timing



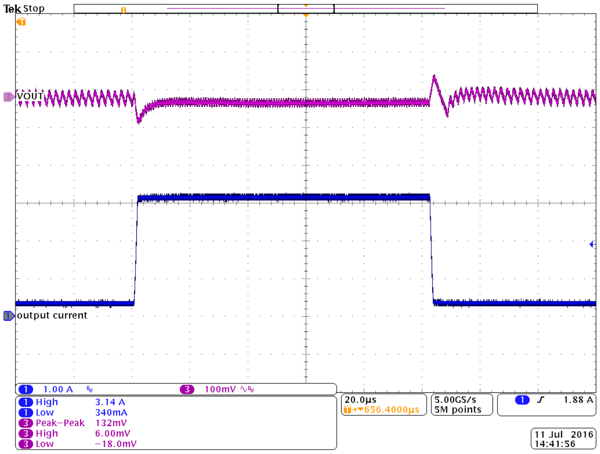
Vin = 5 V; PFM Io = 0.1 A
Vout = 1.2 V T_A= 25 °C

Figure 36. Output Voltage Ripple



Vin = 5 V; PWM Io = 1 A
Vout = 1.2 V T_A= 25 °C

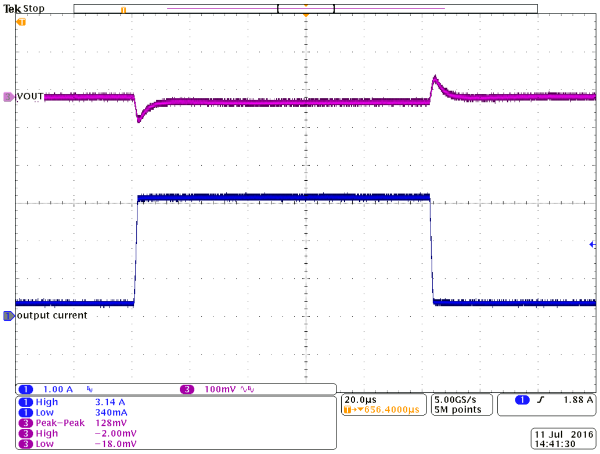
Figure 37. Output Voltage Ripple



Vout = 1.8 V PFM Io = 350 mA to 3.1 A

T_A= 25 °C

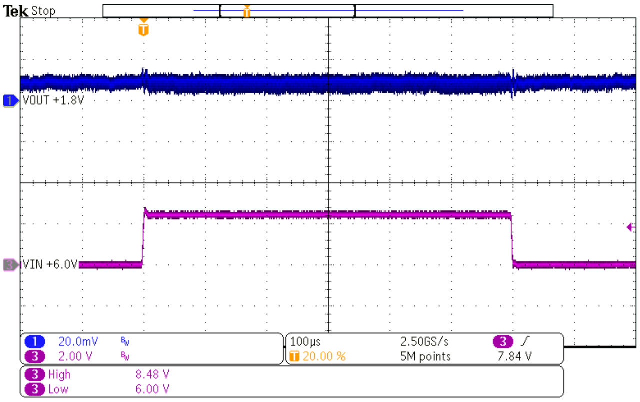
Figure 38. Load Transient Response



Vout = 1.8 V PWM Io = 350 mA to 3.1 A

T_A= 25°C

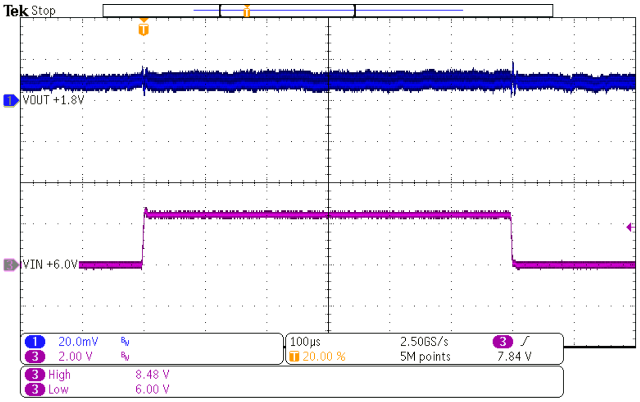
Figure 39. Load Transient Response



Vin = 6 V to 8.4 V; PFM Io = 1 A

Vout = 1.8 V T_A= 25 °C

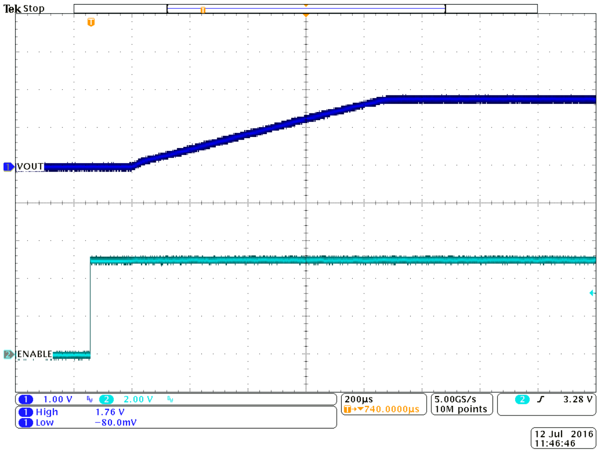
Figure 40. Line Transient Response



Vin = 6 V to 8.4 V; PWM Io = 1 A

Vout = 1.8 V T_A= 25 °C

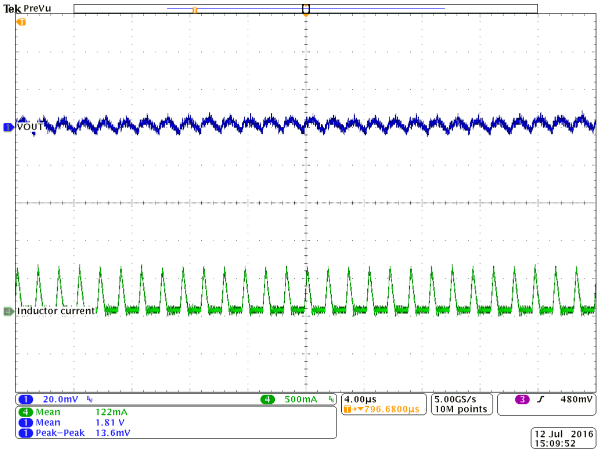
Figure 41. Line Transient Response



Vout = 1.8 V PWM Rload = 1 kΩ

T_A= 25 °C

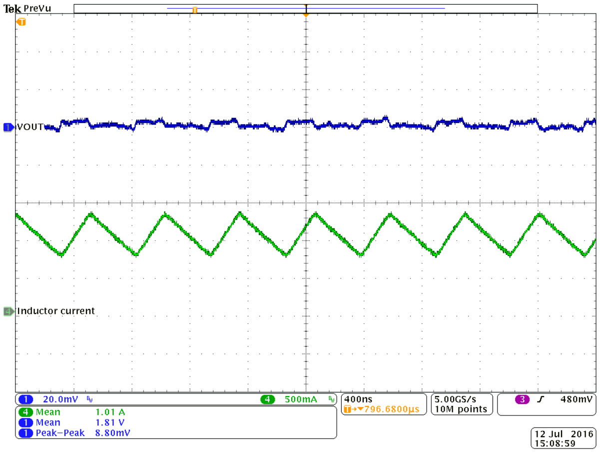
Figure 42. Start-Up Timing



Vout = 1.8 V PFM Io = 0.1 A

T_A= 25 °C

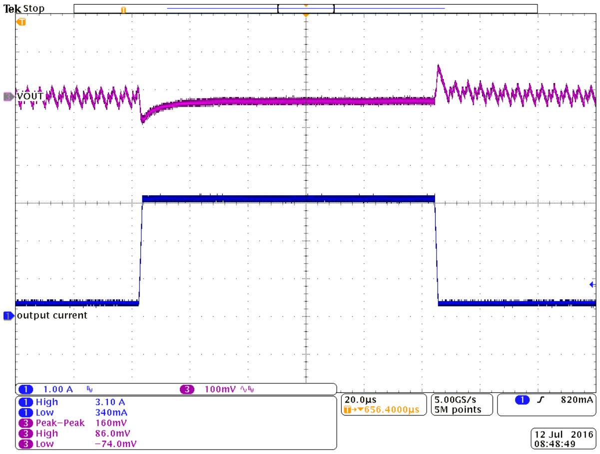
Figure 43. Output Voltage Ripple



Vout = 1.8 V PWM Io = 1 A

T_A= 25 °C

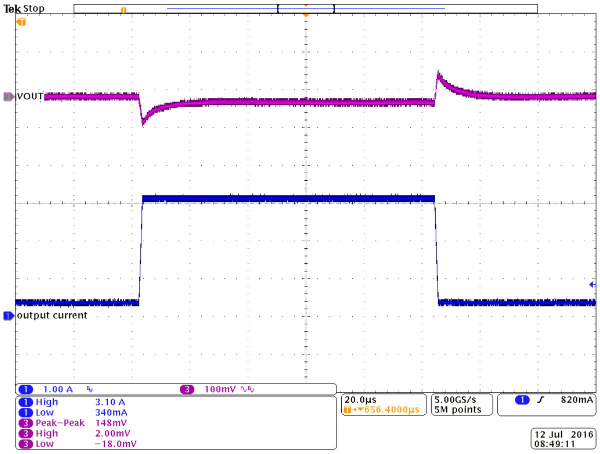
Figure 44. Output Voltage Ripple



Vout = 3.3 V PFM Io = 350 mA to 3.1 A

T_A= 25 °C

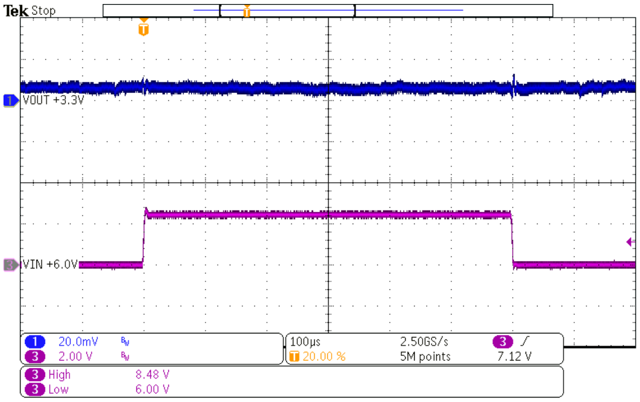
Figure 45. Load Transient Response



Vout = 3.3 V PWM Io = 350 mA to 3.1 A

T_A= 25 °C

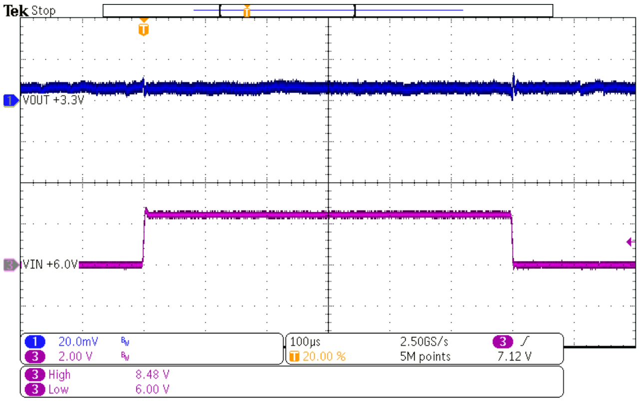
Figure 46. Load Transient Response



Vin = 6 V to 8.4 V; PFM Io = 1 A

Vout = 3.3 V T_A= 25 °C

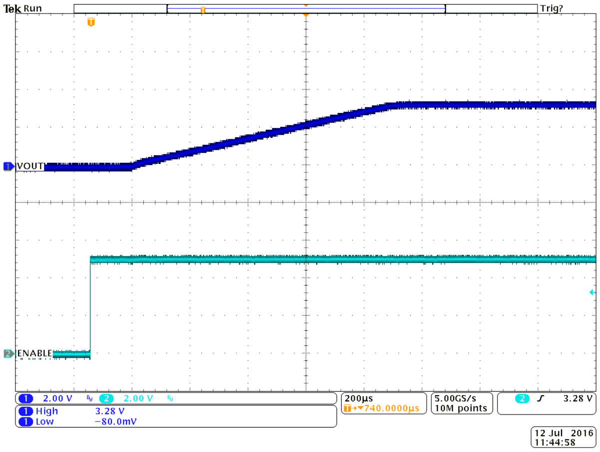
Figure 47. Line Transient Response



Vin = 6 V to 8.4 V; PWM Io = 1 A

Vout = 3.3 V T_A= 25 °C

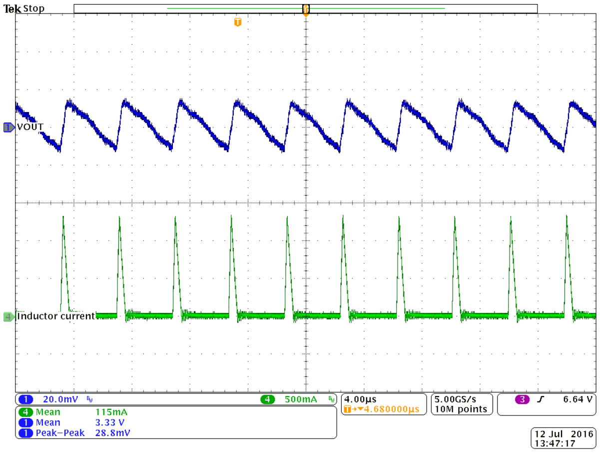
Figure 48. Line Transient Response



Vout = 3.3 V PWM Rload = 1 kΩ

T_A= 25 °C

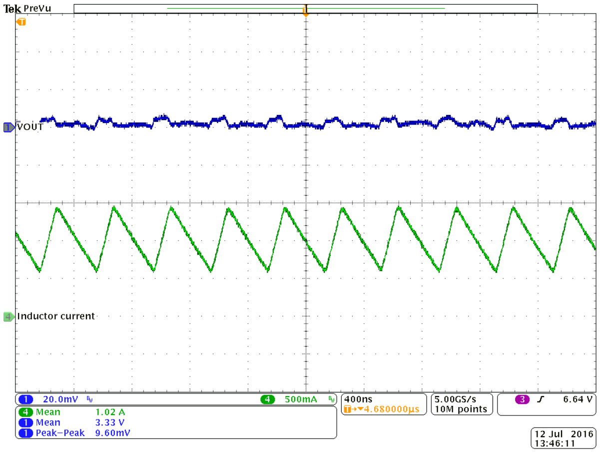
Figure 49. Start-Up Timing



Vout = 3.3 V PFM Io = 0.1 A

T_A= 25 °C

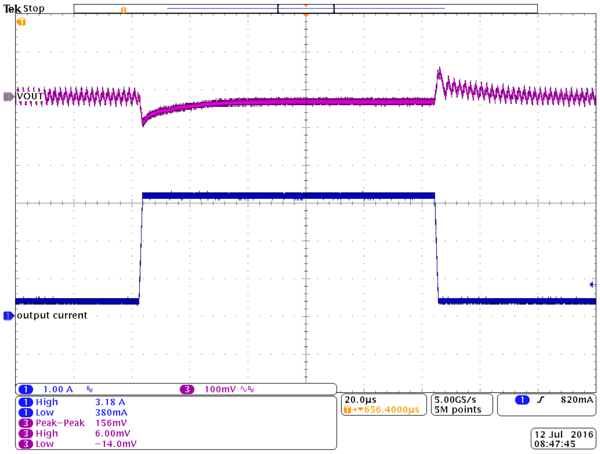
Figure 50. Output Voltage Ripple



Vout = 3.3 V PWM Io = 1 A

T_A= 25 °C

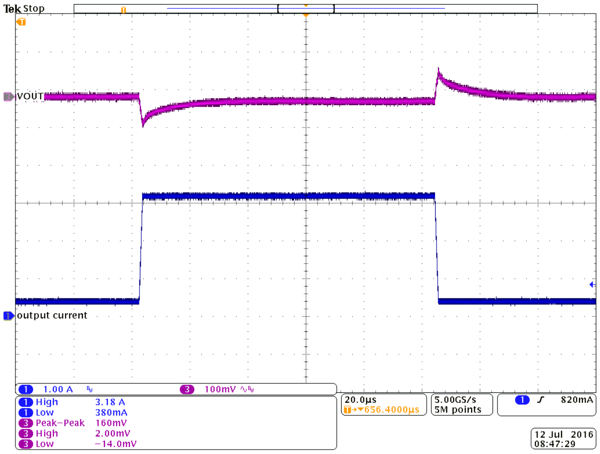
Figure 51. Output Voltage Ripple



Vout = 5 V PFM Io = 350 mA to 3.1 A

T_A= 25 °C

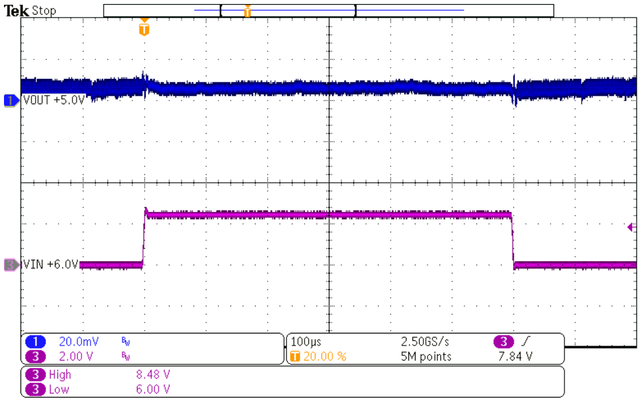
Figure 52. Load Transient Response



Vout = 5 V PWM Io = 350 mA to 3.1 A

T_A= 25 °C

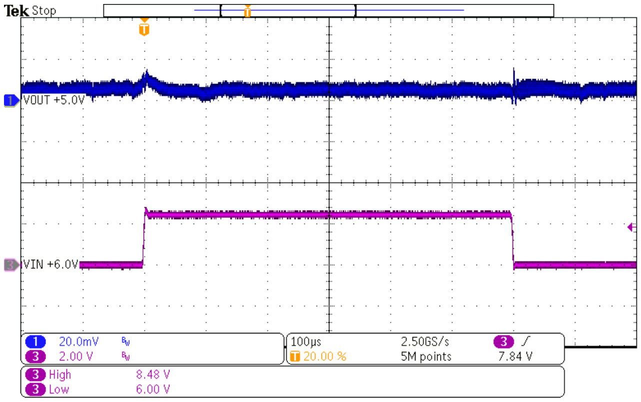
Figure 53. Load Transient Response



Vin = 6 V to 8.4 V; PFM Io = 1 A

Vout = 5 V T_A= 25 °C

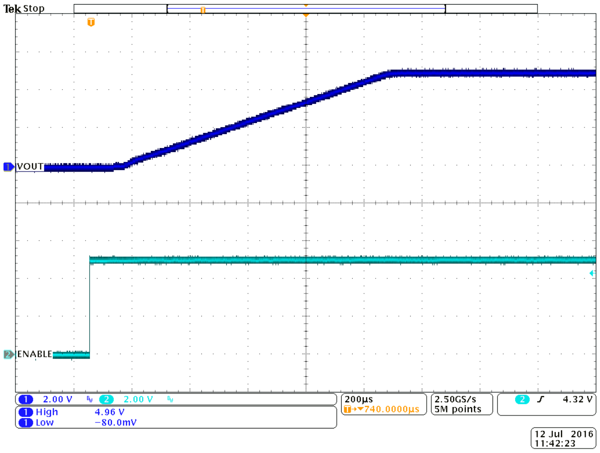
Figure 54. Line Transient Response



Vin = 6 V to 8.4 V; PWM Io = 1 A

Vout = 5 V T_A= 25 °C

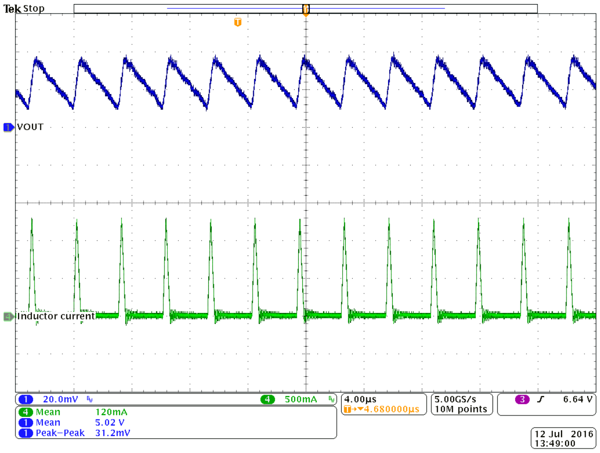
Figure 55. Line Transient Response



Vout = 5 V PWM Rload = 1 kΩ

T_A= 25 °C

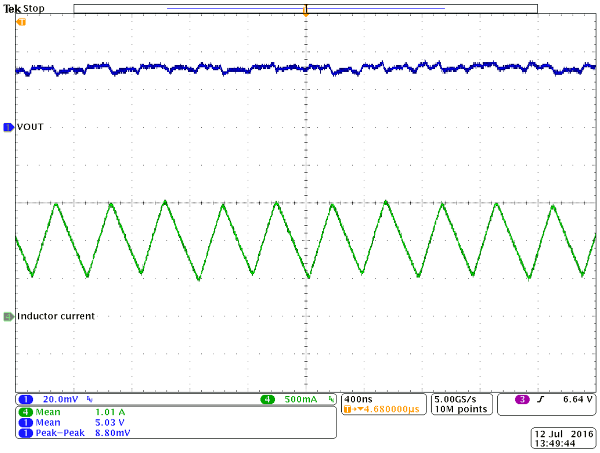
Figure 56. Start-Up Timing



Vout = 5 V PFM Io = 0.1 A

T_A= 25 °C

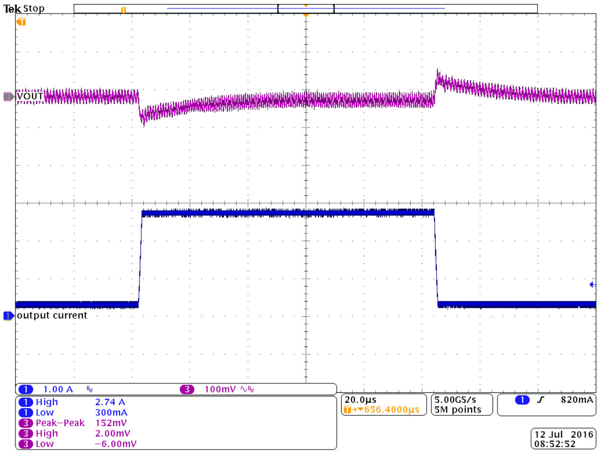
Figure 57. Output Voltage Ripple



Vout = 5 V PWM Io = 1 A

T_A= 25 °C

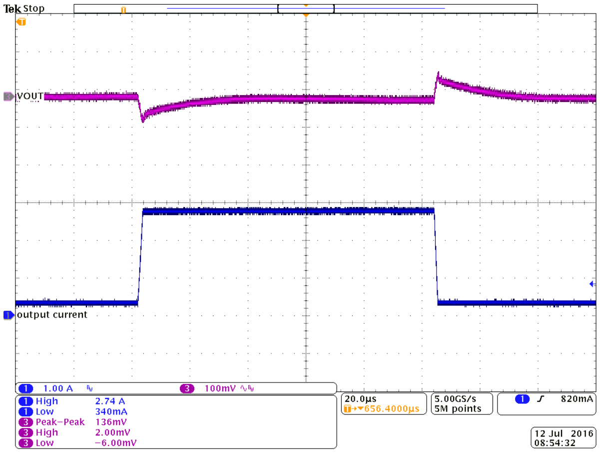
Figure 58. Output Voltage Ripple



Vout = 9 V PFM Io = 300 mA to 2.7 A

T_A= 25 °C

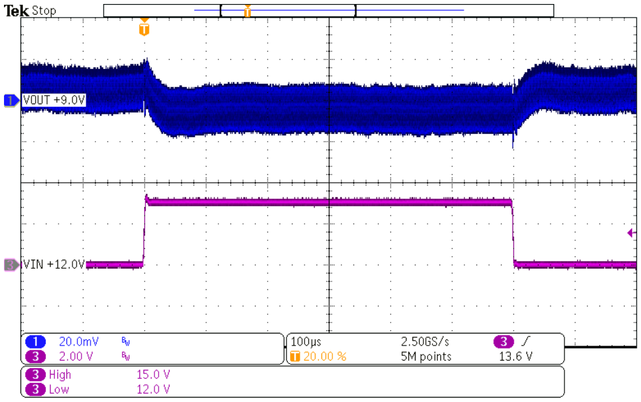
Figure 59. Load Transient Response



Vout = 9 V PWM Io = 300 mA to 2.7 A

T_A= 25 °C

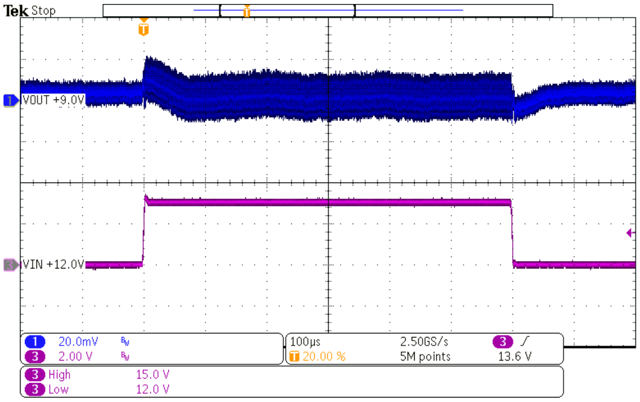
Figure 60. Load Transient Response



Vin = 12 V to 15 V; PFM Io = 1 A

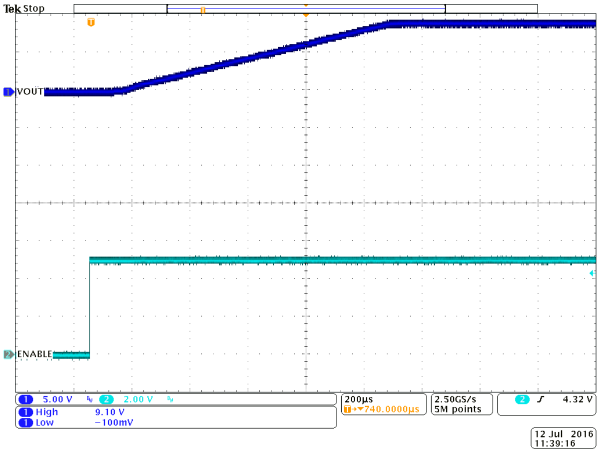
Vout = 9 V T_A= 25 °C

Figure 61. Line Transient Response



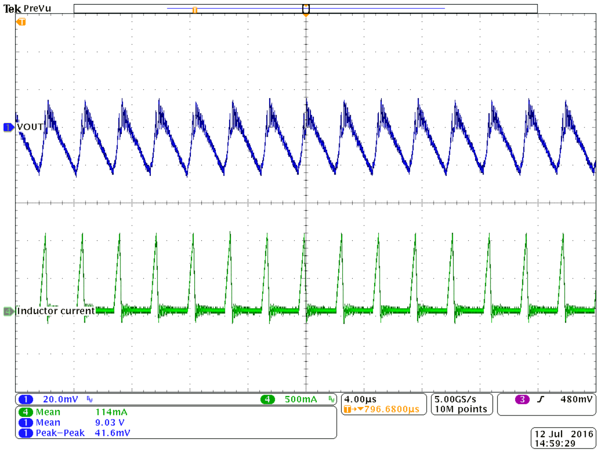
Vin = 12 V to 15 V; PWM Io = 1 A
Vout = 9 V T_A= 25 °C

Figure 62. Line Transient Response



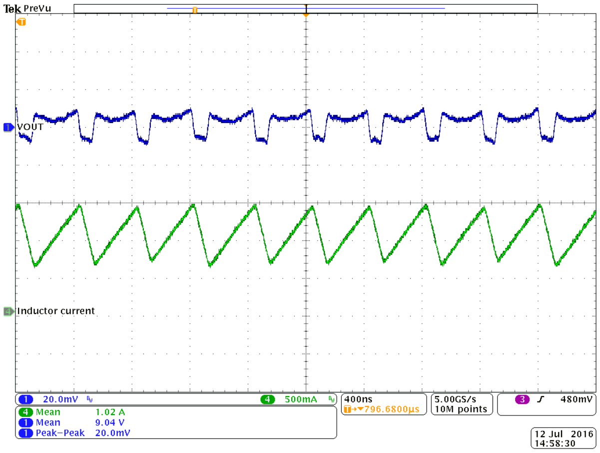
Vout = 9 V PWM Rload = 1 kΩ
T_A= 25 °C

Figure 63. Start-Up Timing



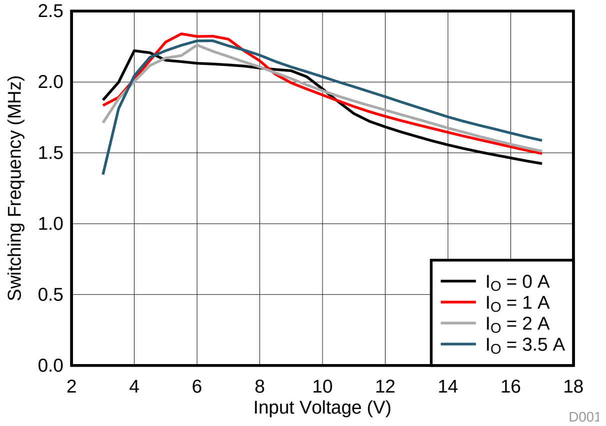
Vout = 9 V PFM Io = 0.1 A
T_A= 25 °C

Figure 64. Output Voltage Ripple



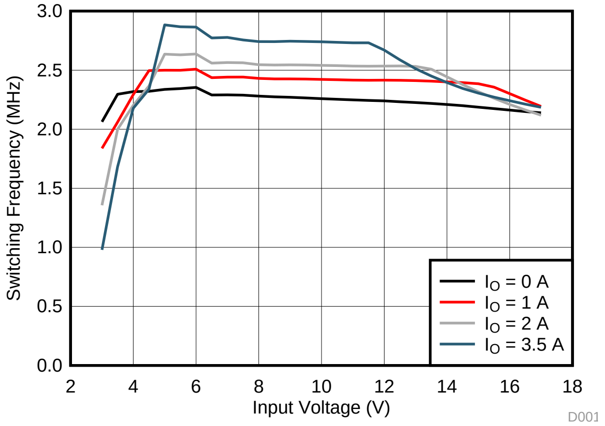
Vout = 9 V PWM Io = 1 A
T_A= 25 °C

Figure 65. Output Voltage Ripple



Vout = 1.2 V PWM T_A= 25 °C

Figure 66. Switching Frequency vs Input Voltage



Vout = 1.8 V PWM T_A= 25 °C

Figure 67. Switching Frequency vs Input Voltage

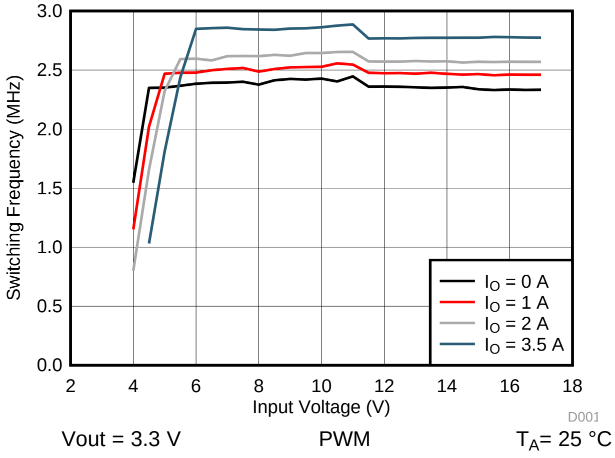


Figure 68. Switching Frequency vs Input Voltage

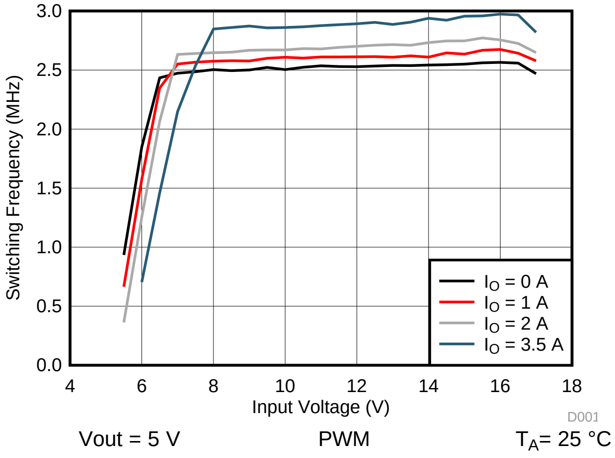


Figure 69. Switching Frequency vs Input Voltage

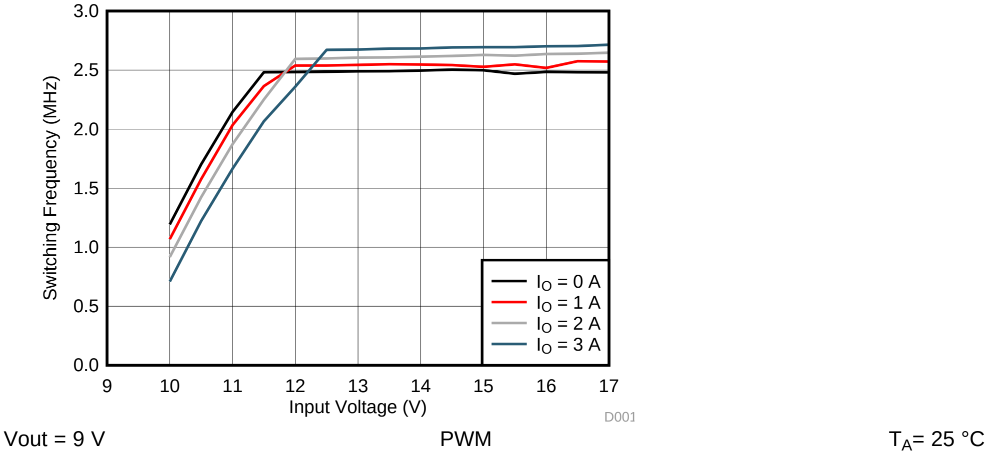


Figure 70. Switching Frequency vs Input Voltage

10.2.2 Typical Application using VSEL and FB2

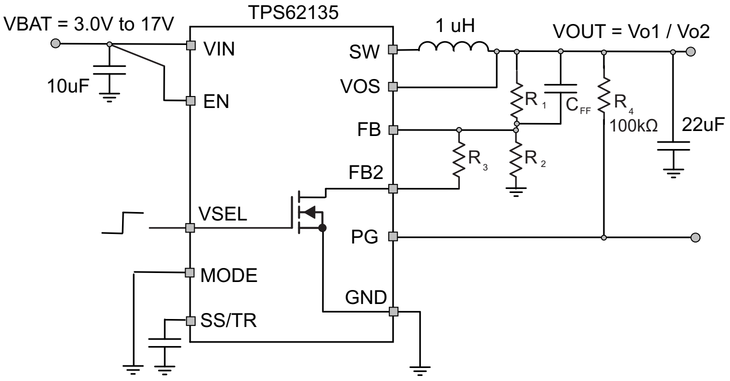


Figure 71. Typical Application using VSEL

10.2.2.1 Design Requirements

VSEL allows to switch between two output voltages by changing the output voltage divider ratio. This is done by an internal MOSFET connecting resistor R3 to GND. Pulling VSEL high turns on the MOSFET that connects R3 in parallel to R2. The divider ratio is changes such that the output voltage increases from Vo1 to Vo2.

When the output voltage is ramped down and the device is in forced PWM mode, the device will sink current.

10.2.2.2 Detailed Design Procedure

TPS62135x typically does not require a feed forward capacitor in parallel to R1. For a large voltage change such as 3.3 V to 5 V, a small feed forward capacitor C_{FF}helps to improve the settling behavior. In order to switch from an output voltage of for example 3.3 V to an output voltage of 5 V, set the resistor divider for R1 and R2 to 3.3V and calculate R3 with Equation 17. With R1 = 560 kΩ and R2 = 150 kΩ this gives R3 = 232 kΩ. A feedforward capacitor of 12 pF was used to get a voltage transition as shown below.

$$R3 = \frac{Vo1 \times R1 \times R2^2}{(Vo2 - Vo1)(R1 \times R2 + R2^2)} \quad for\ Vo2 > Vo1 \tag{17}$$

10.2.2.3 Application Curves

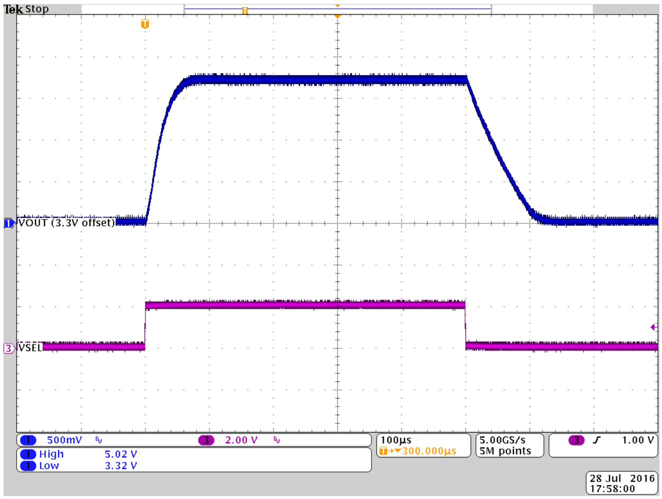


Figure 72. Output Voltage Change from 3.3 V to 5 V in PFM with 20 Ω load resistance

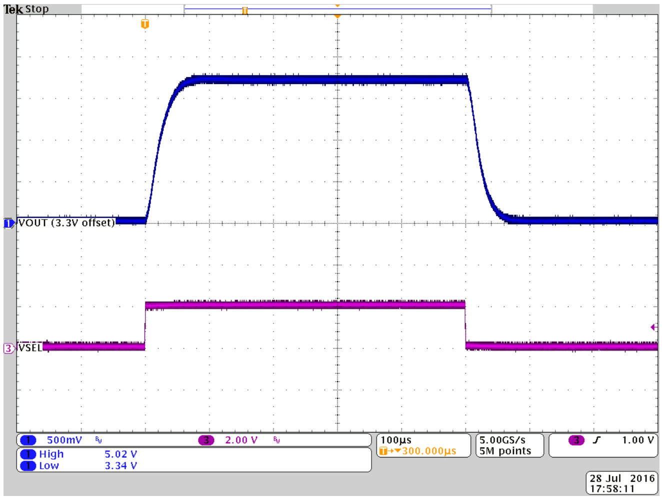


Figure 73. Output Voltage Change from 3.3 V to 5 V in PWM with 20 Ω load resistance

10.3 System Examples

10.3.1 LED Power Supply

The TPS62135x can be used as a power supply for power LEDs. The FB pin can be easily set down to lower values than nominal by using the SS/TR pin. With that, the voltage drop on the sense resistor is low to avoid excessive power loss. Since this pin provides 2.5 µA, the feedback pin voltage can be adjusted by an external resistor per Equation 18. This drop, proportional to the LED current, is used to regulate the output voltage (anode voltage) to a proper level to drive the LED. Both analog and PWM dimming are supported with the TPS62135x. Figure 74 shows an application circuit, tested with analog dimming:

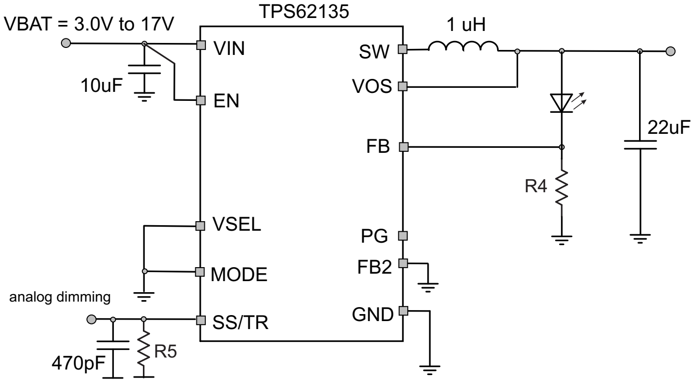


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Figure 74. Single Power LED Supply

The resistor at SS/TR defines the FB voltage. It is set to 350 mV by R5 = 140 kΩ using Equation 18. This cuts the losses on R4 to half from the nominal 0.7 V of feedback voltage while it still provides good accuracy.

$$V_{FB} = 2.5\mu A \times R_{SS/TR} + 11mV \quad (18)$$

The device now supplies a constant current set by resistor R4 from FB to GND. The minimum input voltage has to be rated according the forward voltage needed by the LED used. More information is available in the Application Note SLVA451.

10.3.2 Powering Multiple Loads

In applications where TPS62135x is used to power multiple load circuits, it may be the case that the total capacitance on the output is very large. In order to properly regulate the output voltage, there needs to be an appropriate AC signal level on the VOS pin. Tantalum capacitors have a large enough ESR to keep output voltage ripple sufficiently high on the VOS pin. With low ESR ceramic capacitors, the output voltage ripple may get very low, so it is not recommended to use a large capacitance directly on the output of the device. If there are several load circuits with their associated input capacitor on a pcb, these loads are typically distributed across the board. This adds enough trace resistance (R_{trace}) to keep a large enough AC signal on the VOS pin for proper regulation.

The minimum total trace resistance on the distributed load is 10 mΩ. The total capacitance n x Cin in the use case below was 32 x 47 uF of ceramic X7R capacitors.

System Examples (continued)

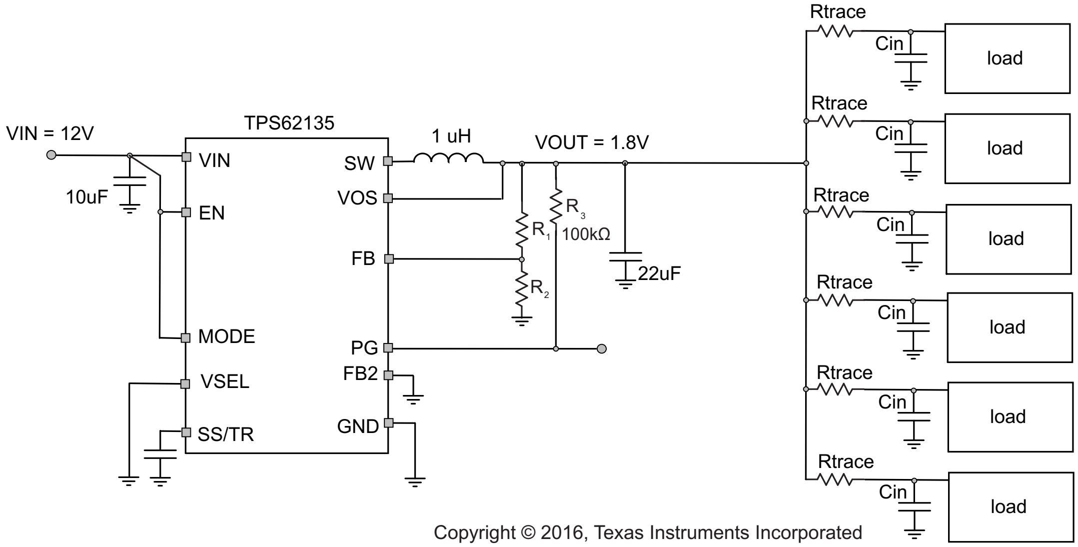

Figure 75. Multiple Loads

10.3.3 Voltage Tracking

DEVICE 2 follows the voltage applied to the SS/TR pin. A ramp on SS/TR to 0.7 V ramps the output voltage according to the 0.7 V reference.

Tracking the 3.3 V of DEVICE 1 requires a resistor divider on SS/TR of DEVICE 2 equal to the output voltage divider of DEVICE 1.

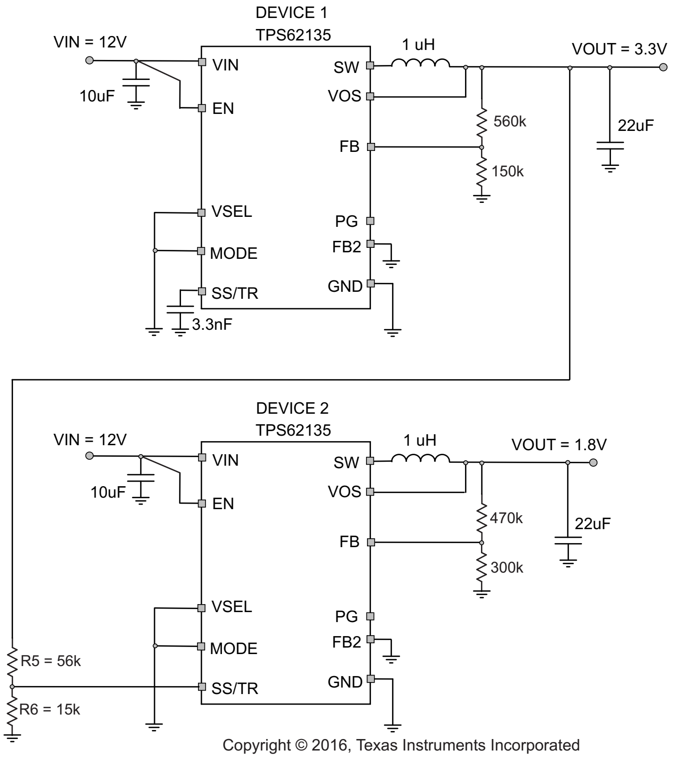

Figure 76. Tracking Example

System Examples (continued)

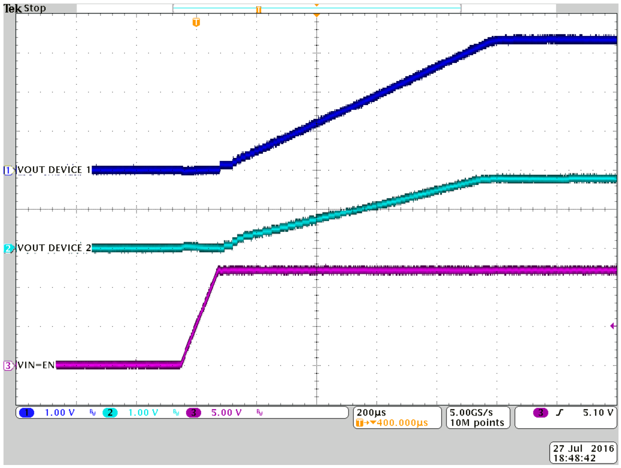

Figure 77. Tracking

10.3.4 Precise Soft-Start Timing

The SS/TR pin of the TPS62135x can be used for tracking as well as for setting the Soft-Start time. The TPS62135x has one GND terminal which is used for the power ground as well as for the analog ground connection. While starting the device with a load current above approximately 1 A, the noise on the GND connection can lead to a Soft-Start time shorter than calculated. There are two external work arounds as given below.

Adding a 10 kΩ resistor filters the noise on the GND connection and keeps the Soft-Start time at the value calculated.

Figure 79 does not require an external component. It provides a connection to the internal analog ground by using the FB2 pin and its internal NMOS to that node. The internal NMOS needs to be turned ON by setting VSEL = high.

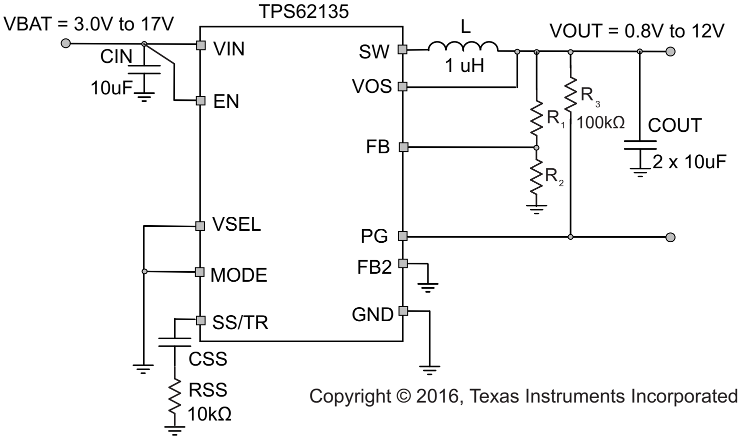

Figure 78. Adding a Series Resistor to CSS

System Examples (continued)

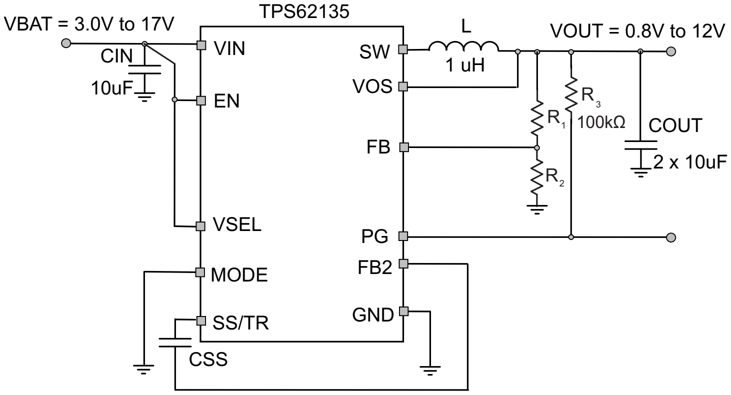

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Figure 79. Connecting CSS to the Internal Analog Ground by using FB2

11 Power Supply Recommendations

The power supply to the TPS62135x needs to have a current rating according to the supply voltage, output voltage, and output current of the TPS62135x.

12 Layout

12.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS62135x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation and noise sensitivity.

See Figure 80 for the recommended layout of the TPS62135x, which is designed for common external ground connections. The input capacitor should be placed as close as possible between the VIN and GND pin of TPS62135x. Also connect the VOS pin in the shortest way to VOUT at the output capacitor.

Provide low inductive and resistive paths for loops with high di/dt. Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths (with respect to all other nodes) for wires with high dv/dt. Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

Sensitive nodes like FB and VOS need to be connected with short wires and not nearby high dv/dt signals (for example SW). As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). The capacitor on the SS/TR pin as well as the FB resistors, R1 and R2, should be kept close to the IC and connect directly to those pins and the system ground plane. The same applies to R3 if FB2 is used to scale the output voltage.

The package uses the pins for power dissipation. Thermal vias on the VIN, GND and SW pins help to spread the heat through the pcb.

In case any of the digital inputs EN, VSEL or MODE need to be tied to the input supply voltage at VIN, the connection must be made directly at the input capacitor as indicated in the schematics.

The recommended layout is implemented on the EVM and shown in its User's Guide, SLVUAI7.

12.2 Layout Example

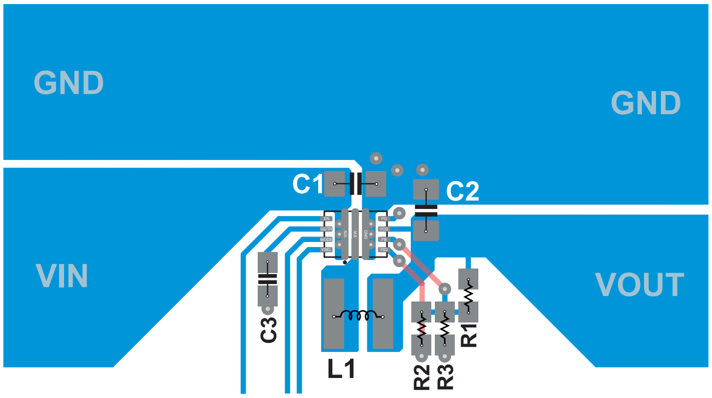

Figure 80. Layout

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design, for example, increasing copper thickness, thermal vias, number of layers
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: Thermal Characteristics Application Note (SZZA017), and (SPRA953).

The TPS62135x is designed for a maximum operating junction temperature (T_J) of 125 °C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, it's recommended to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62135	Click here	Click here	Click here	Click here	Click here
TPS621351	Click here	Click here	Click here	Click here	Click here

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13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS621351RGXR	PREVIEW	VQFN-HR	RGX	11	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	621351	
TPS621351RGXT	PREVIEW	VQFN-HR	RGX	11	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	621351	
TPS62135RGXR	PREVIEW	VQFN-HR	RGX	11	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	62135	
TPS62135RGXT	PREVIEW	VQFN-HR	RGX	11	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	62135	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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