

## NCE N-Channel Enhancement Mode Power MOSFET

### Description

The NCE3050K uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

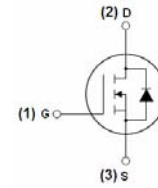
### General Features

- $V_{DS} = 30V, I_D = 50A$   
 $R_{DS(ON)} < 11m\Omega @ V_{GS}=10V$  (Typ:8m $\Omega$ )  
 $R_{DS(ON)} < 16m\Omega @ V_{GS}=4.5V$  (Typ:10m $\Omega$ )
- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible Power Supply

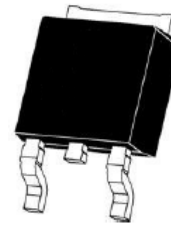
**100% UIS TESTED!**  
**100%  $\Delta V_d$ s TESTED!**



Schematic diagram



Marking and pin assignment



TO-252-2L top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE3050K	NCE3050K	TO-252-2L	-	-	-

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	50	A
Drain Current-Continuous( $T_C=100^\circ C$ )	$I_D(100^\circ C)$	35.4	A
Pulsed Drain Current	$I_{DM}$	200	A
Maximum Power Dissipation	$P_D$	60	W
Drain Source voltage slope, $V_{DS} \leq 24 V$ ,	$dv/dt$	50	V/ns
Drain Source voltage slope, $V_{DS} \leq 24 V, I_{SD} < I_D$	$dv/dt$	50	V/ns
Derating factor		0.4	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	100	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

### Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	2.5	$^\circ C/W$
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**Electrical Characteristics (T<sub>C</sub>=25°C unless otherwise noted)**

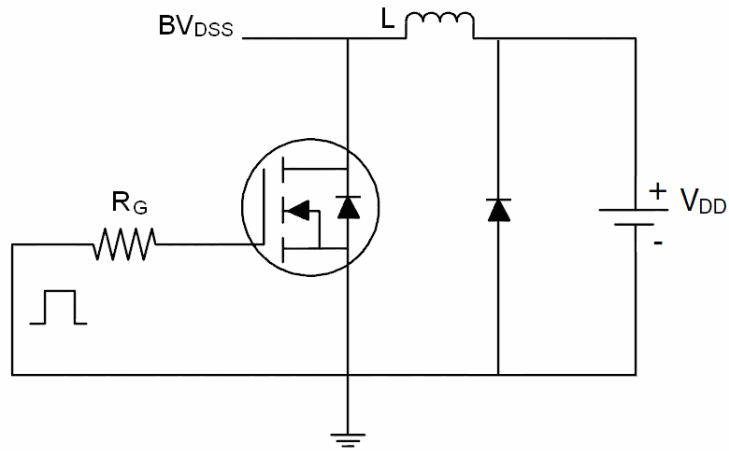
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30	33	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> (Note 3)						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.6	2.6	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	-	8	11	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =20A	-	10	16	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A		20	-	S
<b>Dynamic Characteristics</b> (Note 4)						
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, F=1.0MHz	-	2000	-	PF
Output Capacitance	C <sub>OSS</sub>		-	280	-	PF
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	210	-	PF
<b>Switching Characteristics</b> (Note 4)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =15V, I <sub>D</sub> =20A V <sub>GS</sub> =10V, R <sub>GEN</sub> =1.8Ω	-	10	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	8	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	25	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	5	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =20A, V <sub>GS</sub> =10V	-	32.3	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	4.9	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	6.9	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	0.85	1.2	V
Diode Forward Current	I <sub>S</sub>		-	-	50	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A di/dt = 100A/μs (Note 3)	-	-	27	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	-	20	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

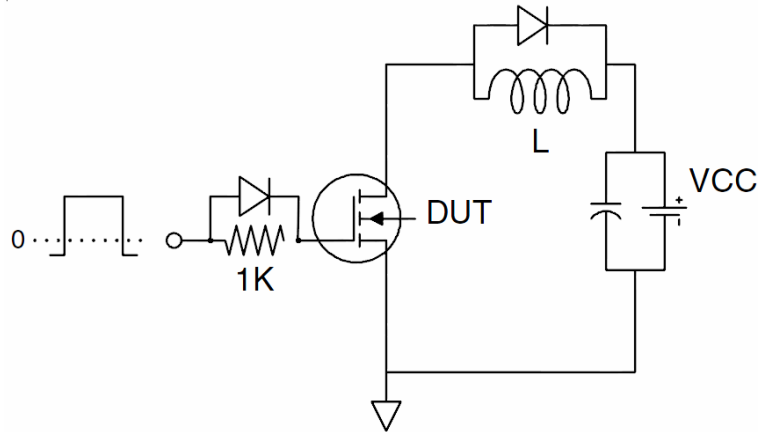
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition: T<sub>J</sub>=25°C, V<sub>DD</sub>=15V, V<sub>G</sub>=10V, L=0.5mH, R<sub>g</sub>=25Ω

## Test circuit

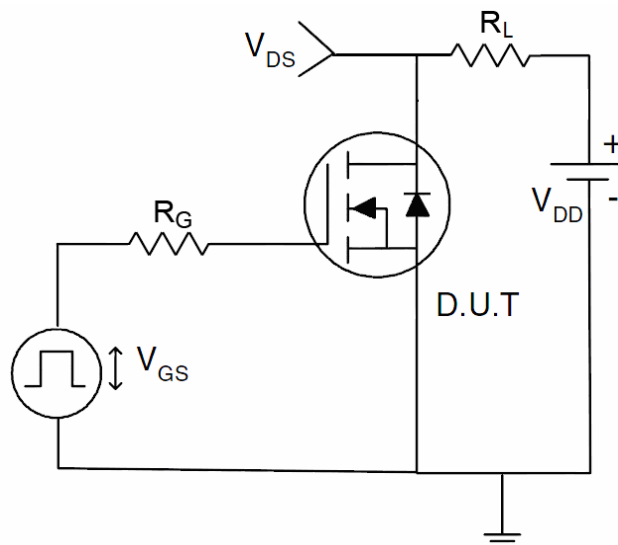
### 1) E<sub>AS</sub> test Circuits



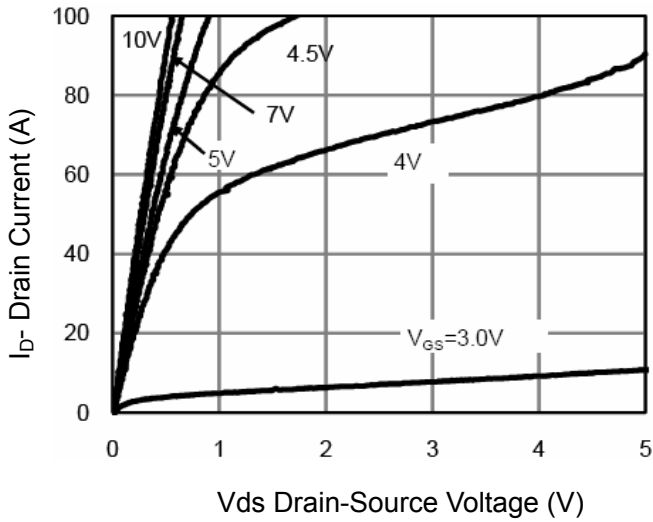
### 2) Gate charge test Circuit:



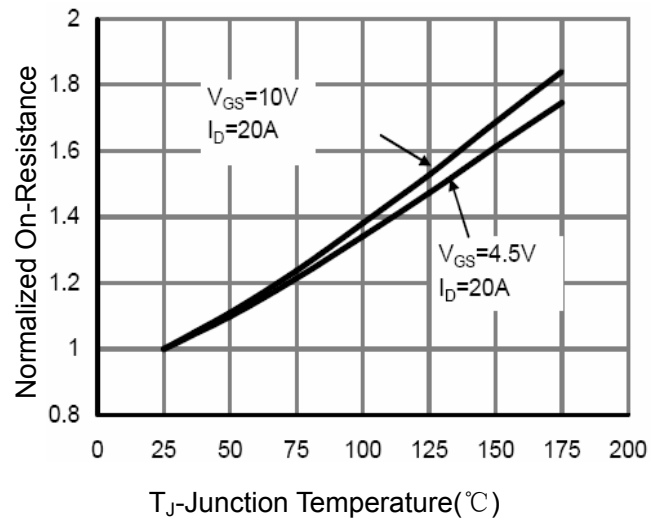
### 3) Switch Time Test Circuit:



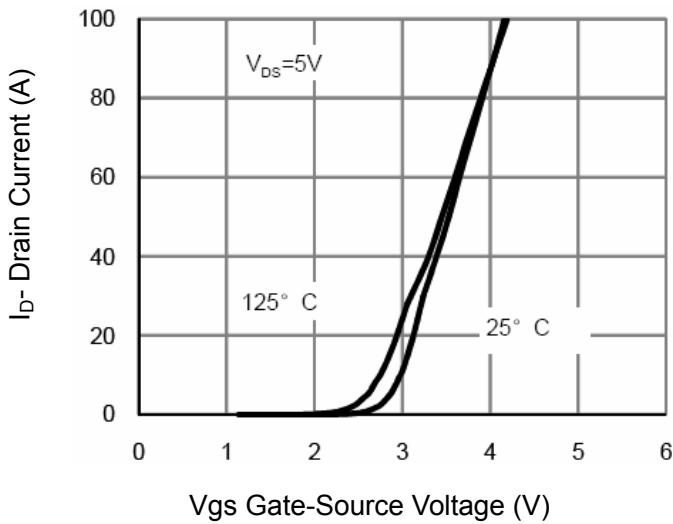
**Typical Electrical and Thermal Characteristics (Curves)**



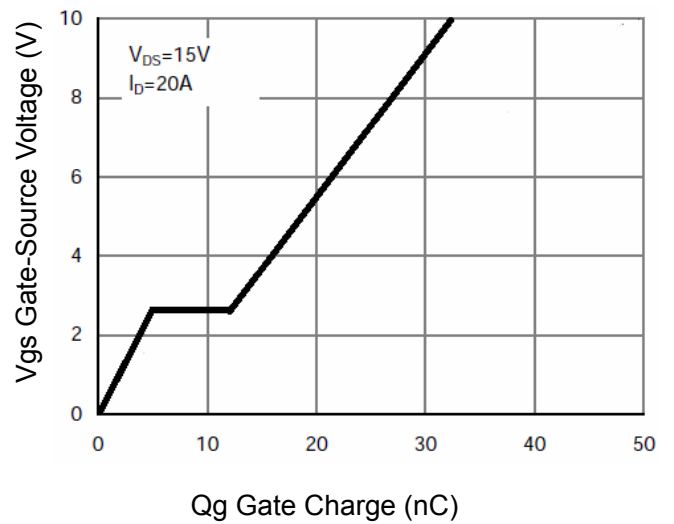
**Figure 1 Output Characteristics**



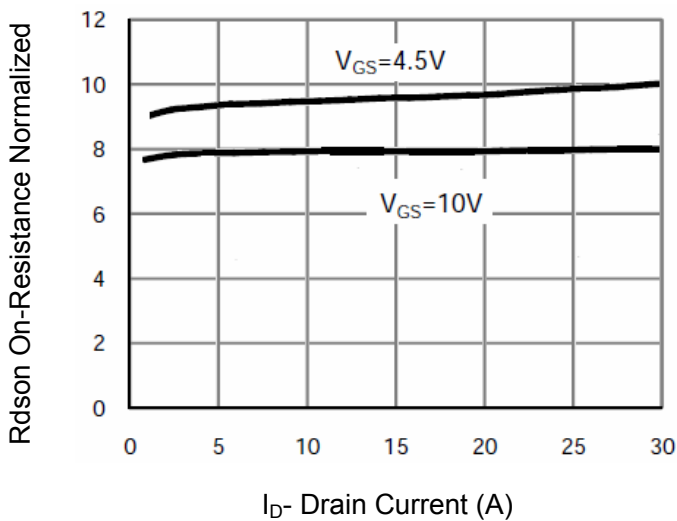
**Figure 4 Rdson-Junction Temperature**



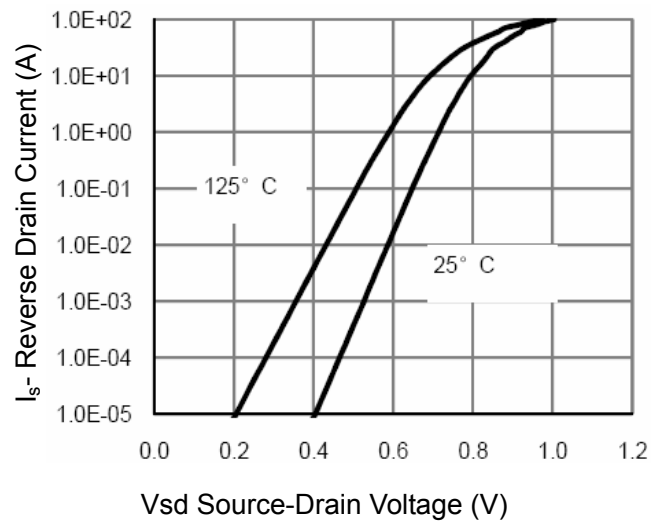
**Figure 2 Transfer Characteristics**



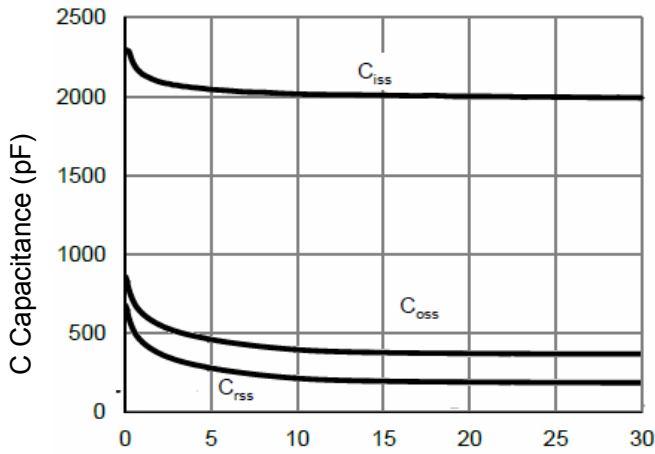
**Figure 5 Gate Charge**



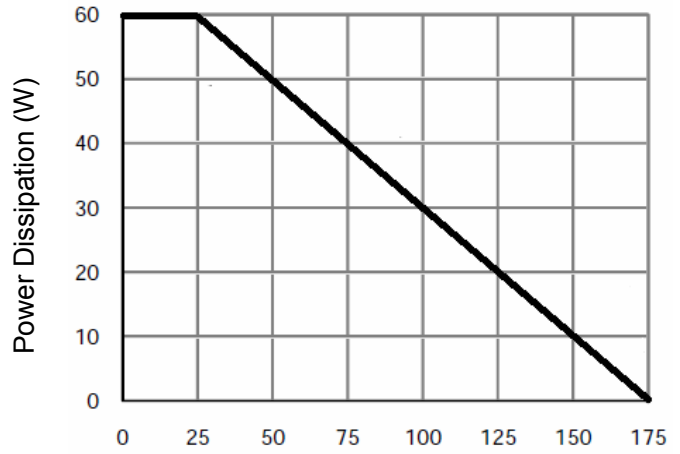
**Figure 3 Rdson- Drain Current**



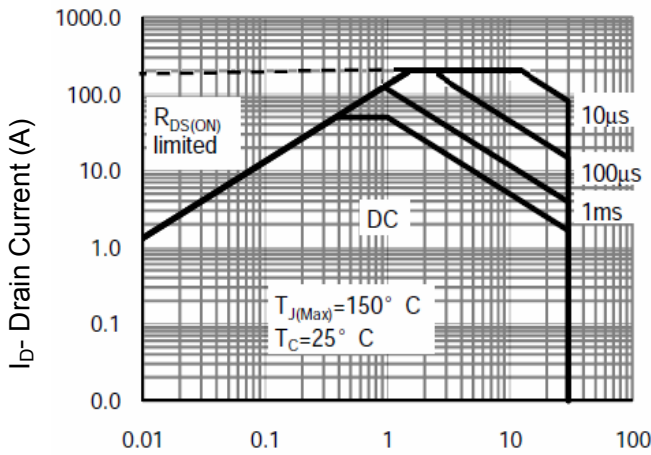
**Figure 6 Source- Drain Diode Forward**



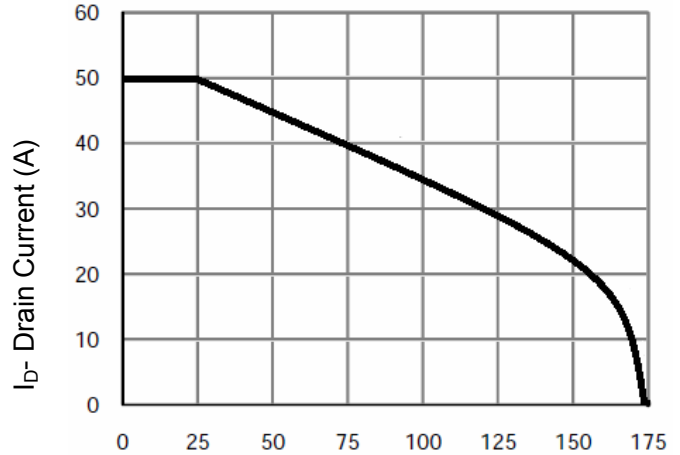
Vds Drain-Source Voltage (V)  
**Figure 7 Capacitance vs Vds**



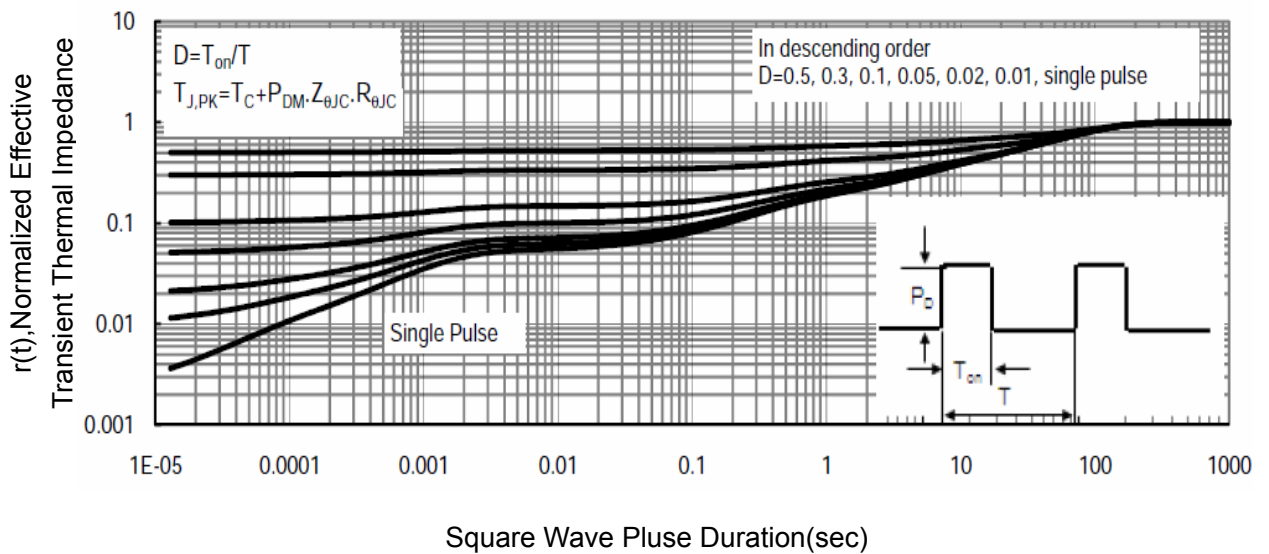
T<sub>J</sub>-Junction Temperature(°C)  
**Figure 9 Power De-rating**



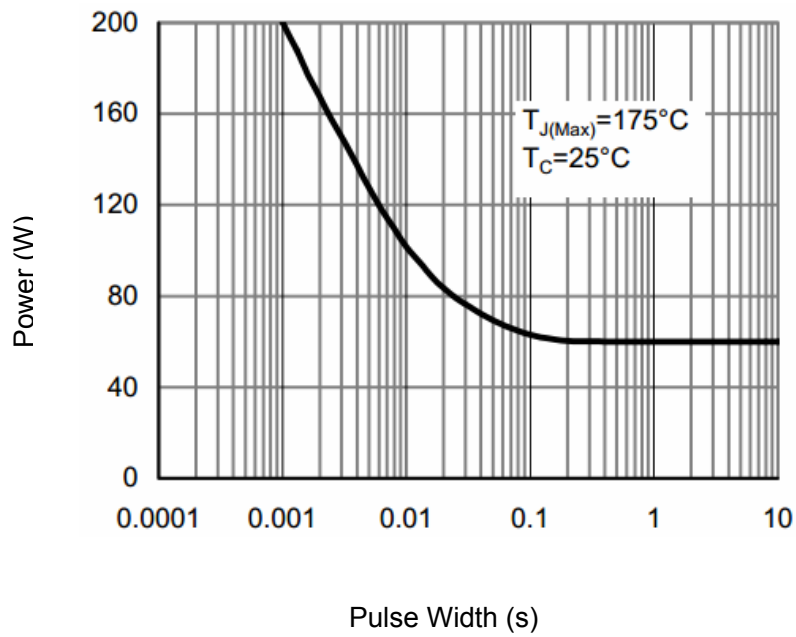
Vds Drain-Source Voltage (V)  
**Figure 8 Safe Operation Area**



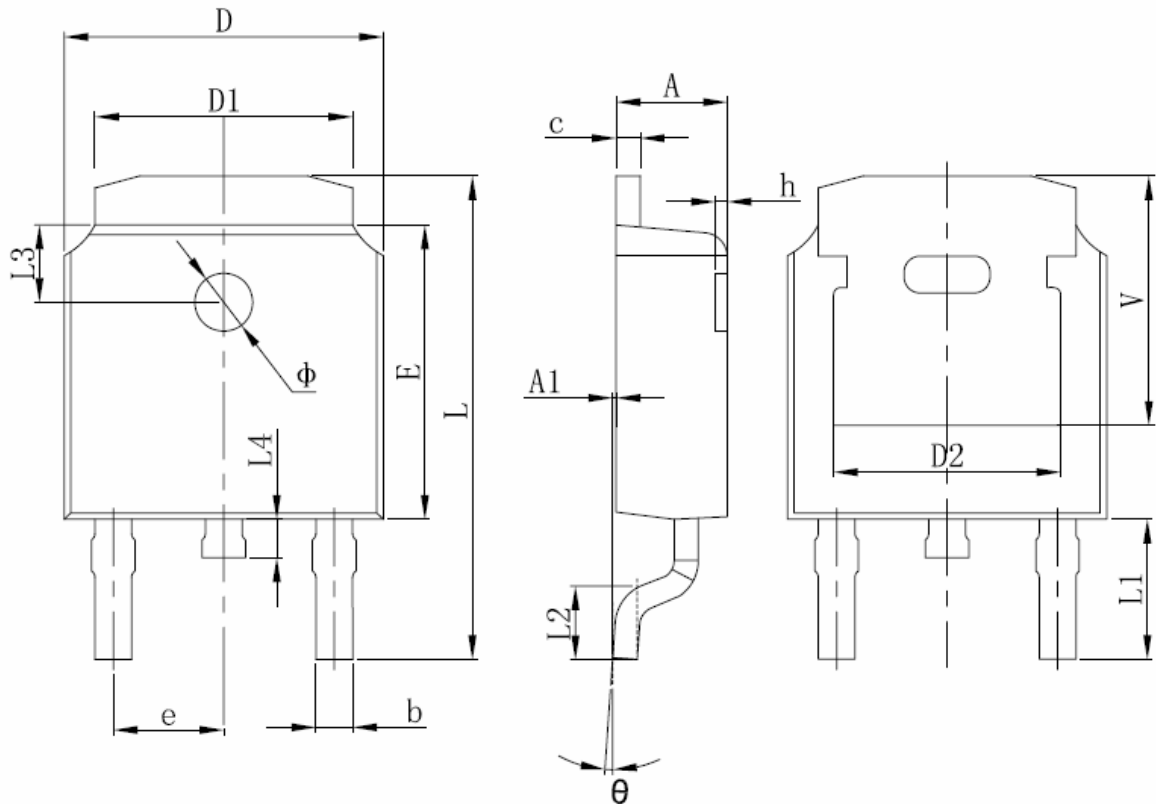
T<sub>J</sub>-Junction Temperature(°C)  
**Figure 10 ID Current- Junction Temperature**



**Figure 11 Normalized Maximum Transient Thermal Impedance**



**Figure 12 Single Pulse Power Rating Junction-to-Ambient**

**TO-252-2L Package Information**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.635	0.770	0.025	0.030
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.712	10.312	0.382	0.406
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.250 REF.		0.207 REF.	

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