

NCE N-Channel Super Trench II Power MOSFET

Description

The NCEP10N85AQ uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

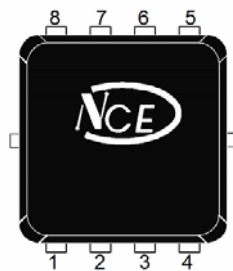
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

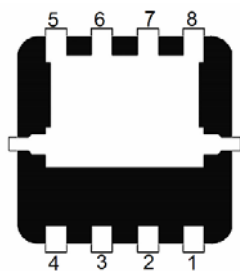
- $V_{DS} = 85V, I_D = 51A$
 $R_{DS(ON)} = 9.5m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 12.5m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!
100% ΔVds TESTED!

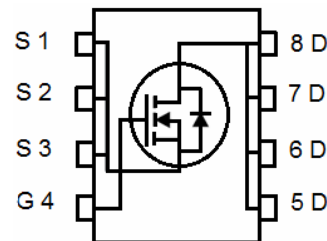
DFN 3.3X3.3



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP10N85AQ	NCEP10N85AQ	DFN3.3X3.3-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	85	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	51	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	37	A
Pulsed Drain Current	I_{DM}	204	A
Maximum Power Dissipation	P_D	56	W
Derating factor		0.45	W/°C
Single pulse avalanche energy ^(Note 5)	E_{AS}	156	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	2.23	°C/W
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Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	85		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=85V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.1	1.7	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=25.5A$	-	9.5	10.0	m Ω
		$V_{GS}=4.5V, I_D=25.5A$	-	12.5	14.0	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=25.5A$	25	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=40V, V_{GS}=0V,$ $F=1.0MHz$	-	1970	-	PF
Output Capacitance	C_{oss}		-	300	-	PF
Reverse Transfer Capacitance	C_{rss}		-	17	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=40V, I_D=25.5A$ $V_{GS}=10V, R_G=3\Omega$	-	16	-	nS
Turn-on Rise Time	t_r		-	18	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	32	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	$V_{DS}=40V, I_D=25.5A,$ $V_{GS}=10V$	-	40	-	nC
Gate-Source Charge	Q_{gs}		-	9.5		nC
Gate-Drain Charge	Q_{gd}		-	9.2		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=25.5A$	-		1.2	V
Diode Forward Current	I_S		-	-	51	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 25.5A$ $di/dt = 100A/\mu s$ (Note 3)	-	45	-	nS
Reverse Recovery Charge	Q_{rr}		-	95	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$
6. The spike duty cycle 5% max, limited by junction temperature $T_J(\text{MAX})=125^\circ\text{C}$

Typical Electrical and Thermal Characteristics

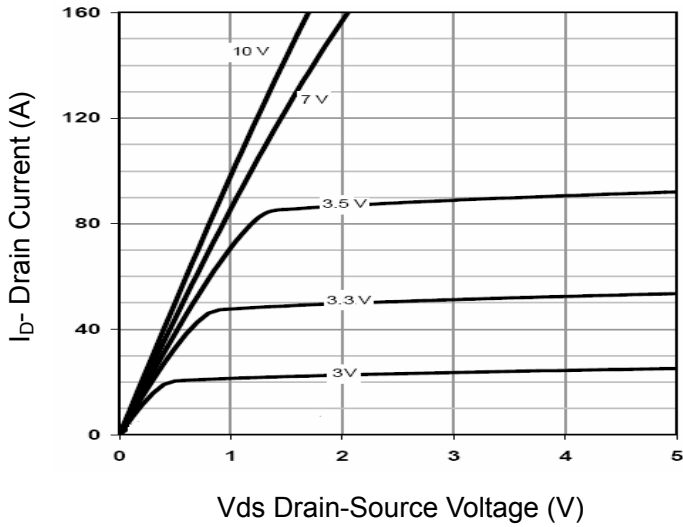


Figure 1 Output Characteristics

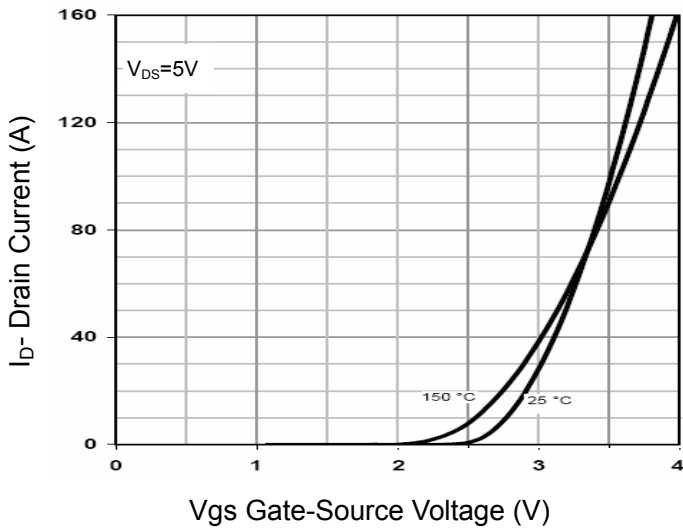


Figure 2 Transfer Characteristics

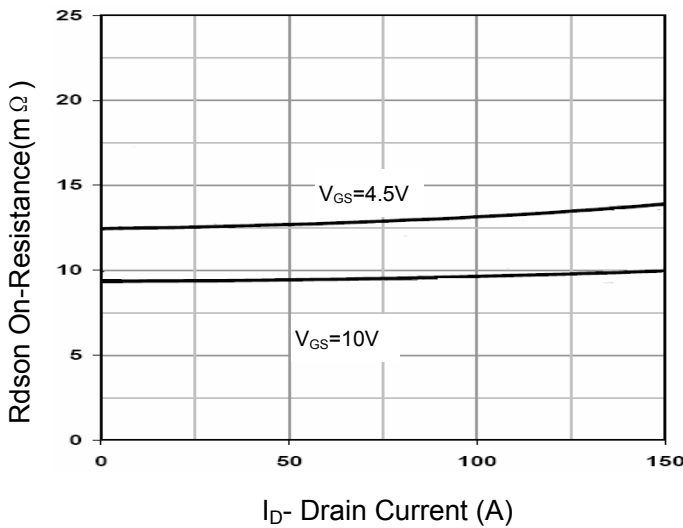


Figure 3 Rdson- Drain Current

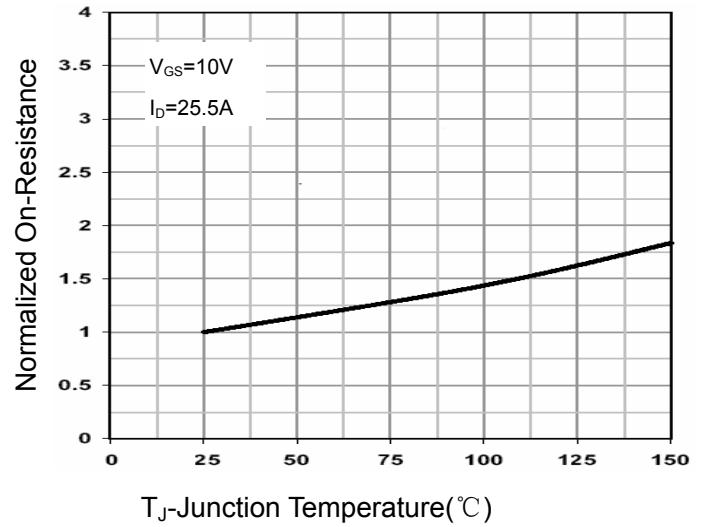


Figure 4 Rdson-Junction Temperature

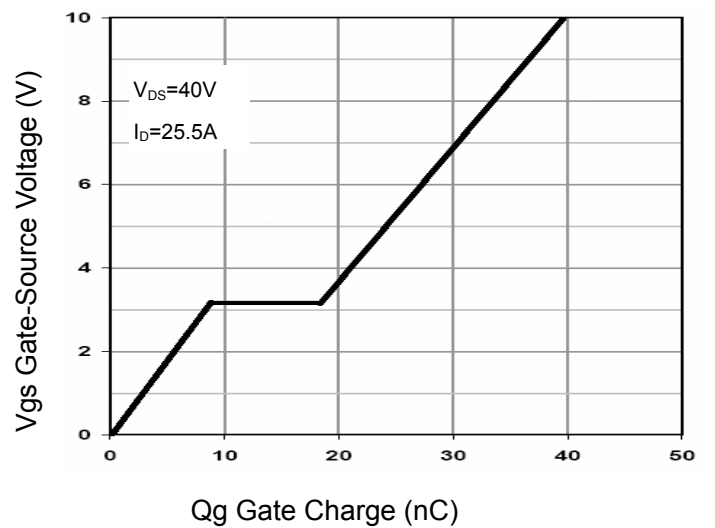


Figure 5 Gate Charge

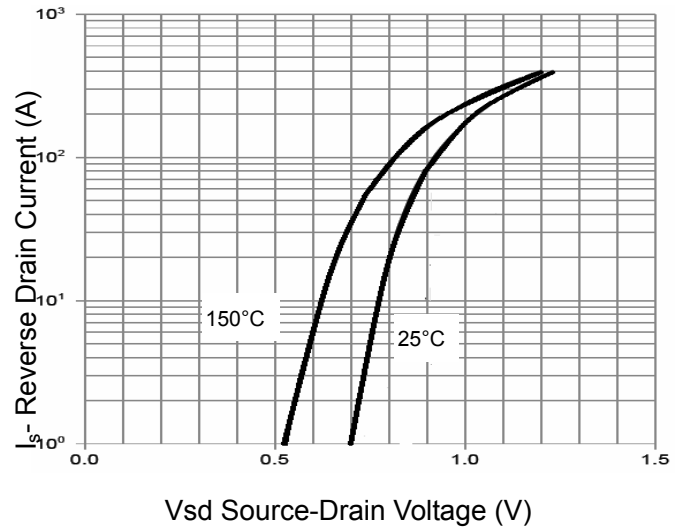
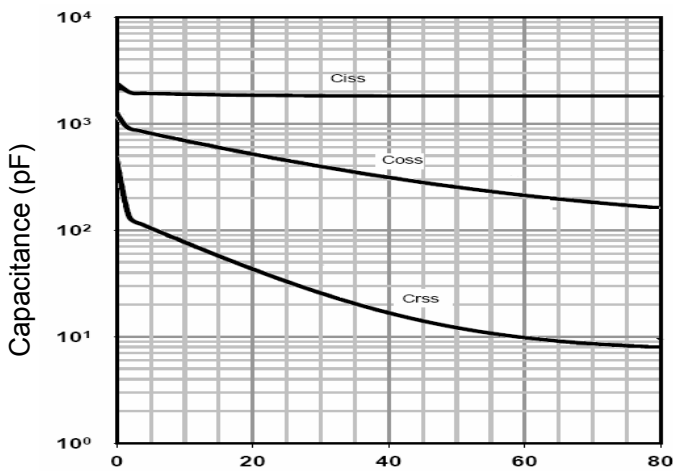
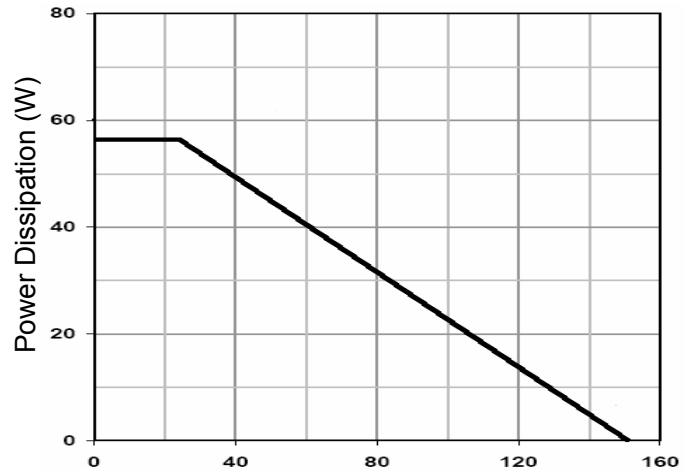


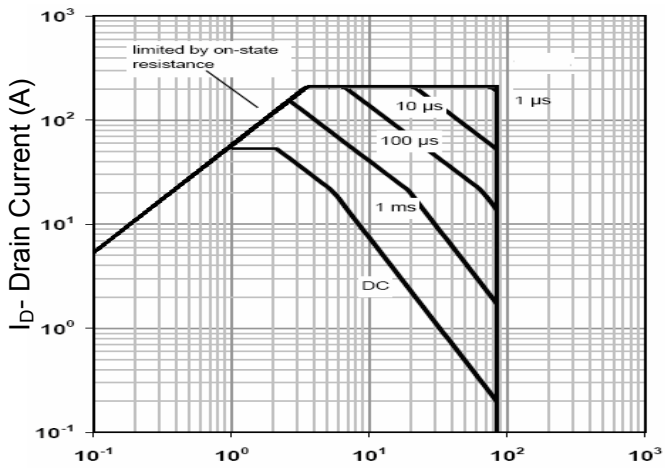
Figure 6 Source- Drain Diode Forward



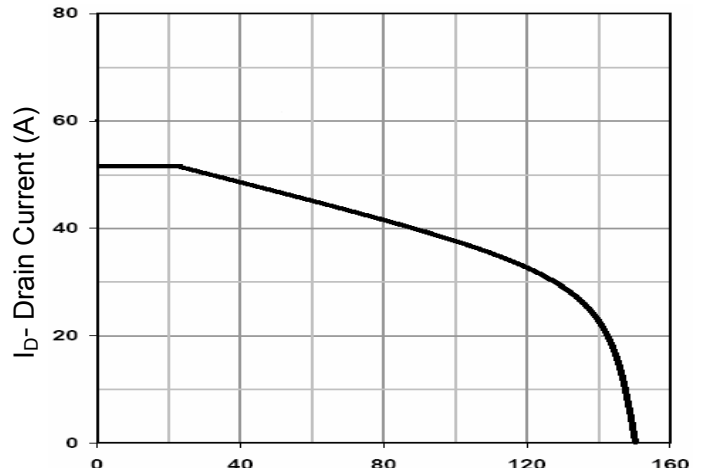
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_C-Case Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_C-Case Temperature (°C)
Figure 10 Current De-rating

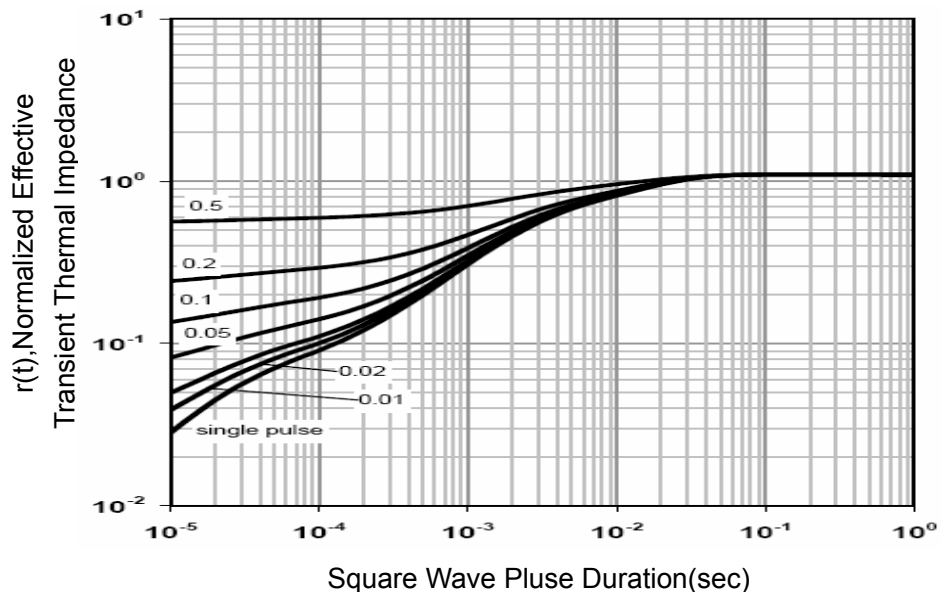
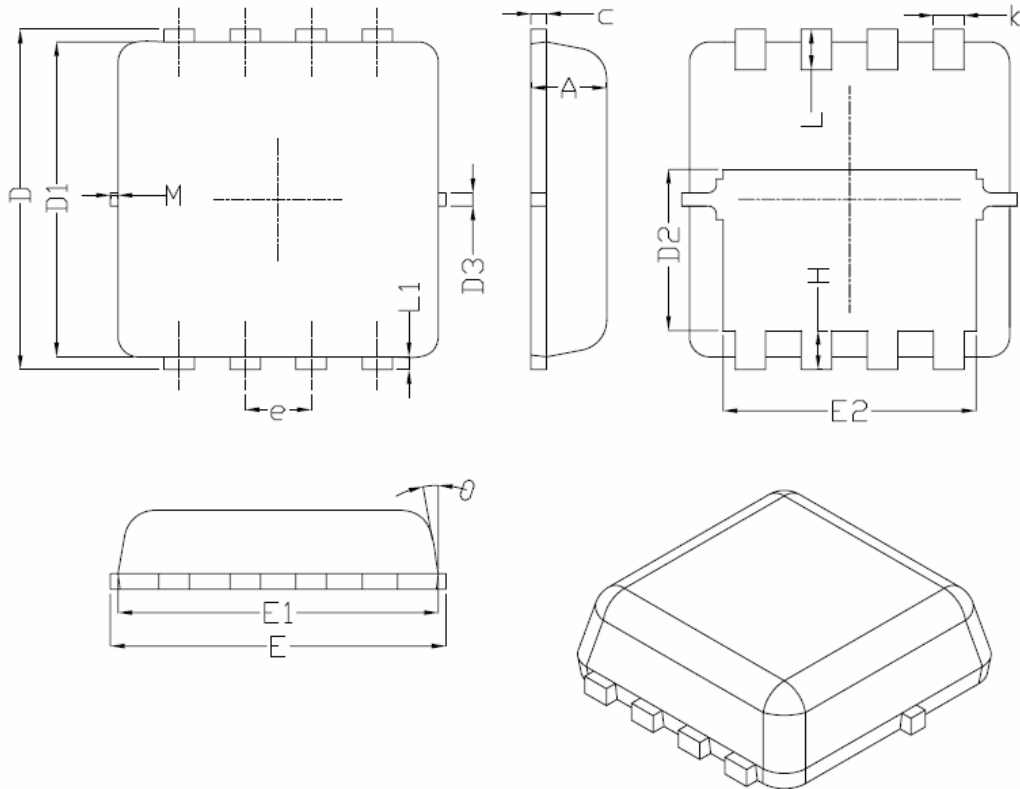


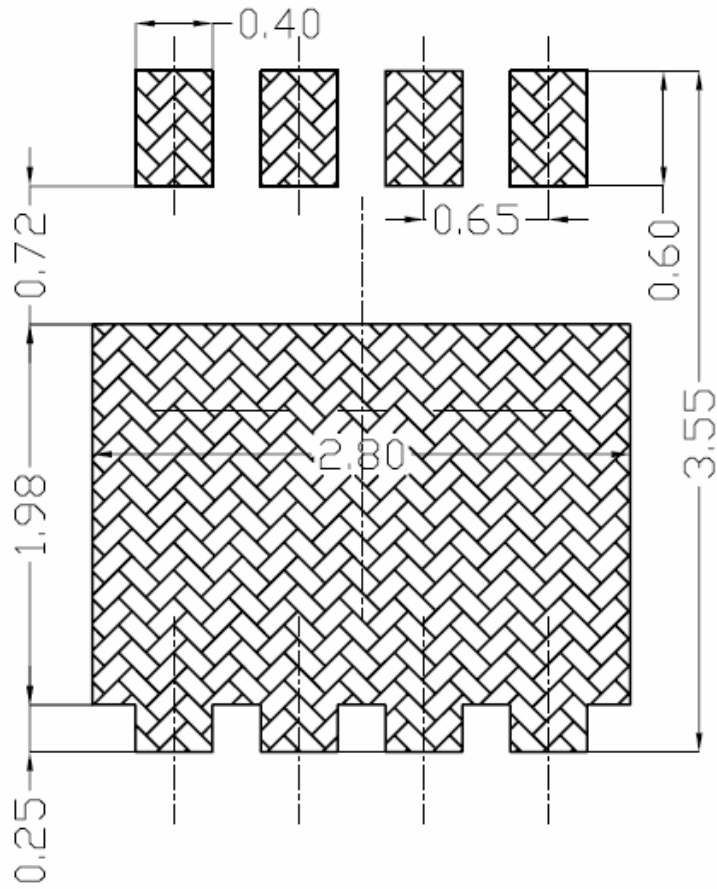
Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3.3X3.3-8L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
θ		10°	12°

Land Pattern (Only for Reference)



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