

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP1216AS uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

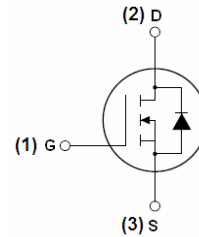
General Features

- $V_{DS} = 120V, I_D = 16A$
 $R_{DS(ON)} = 8.7m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 10.0m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

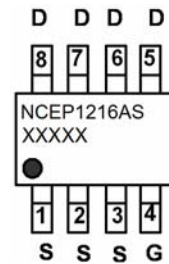
Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

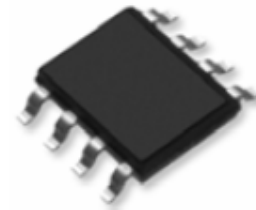
100% UIS TESTED!



Schematic diagram



Marking and pin assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP1216AS	NCEP1216AS	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	120	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	16	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	11.3	A
Pulsed Drain Current	I_{DM}	64	A
Maximum Power Dissipation	P_D	3.5	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	210	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient ^(Note 2)	$R_{\theta JA}$	36	$^\circ C/W$
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

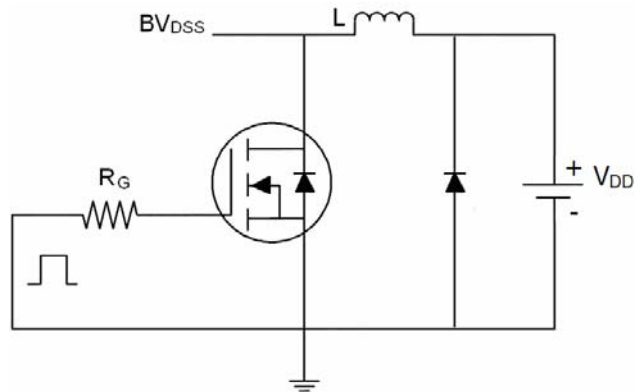
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	120	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=120V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.7	2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=16A$	-	8.7	10.3	m Ω
		$V_{GS}=4.5V, I_D=16A$	-	10.0	10.6	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=16A$	50	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=60V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	4960		PF
Output Capacitance	C_{oss}		-	389		PF
Reverse Transfer Capacitance	C_{rss}		-	25.3		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=60V, I_D=16A$ $V_{GS}=10V, R_G=1.6\Omega$	-	15.4	-	nS
Turn-on Rise Time	t_r		-	9.9	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	42.9	-	nS
Turn-Off Fall Time	t_f		-	5.5	-	nS
Total Gate Charge	Q_g	$V_{DS}=60V, I_D=16A,$ $V_{GS}=10V$	-	63.8	-	nC
Gate-Source Charge	Q_{gs}		-	16.5	-	nC
Gate-Drain Charge	Q_{gd}		-	8.8	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=16A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	16	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = I_S$	-	105	-	nS
Reverse Recovery Charge	Q_{rr}	$di/dt = 100A/\mu s$ (Note 3)	-	200	-	nC

Notes:

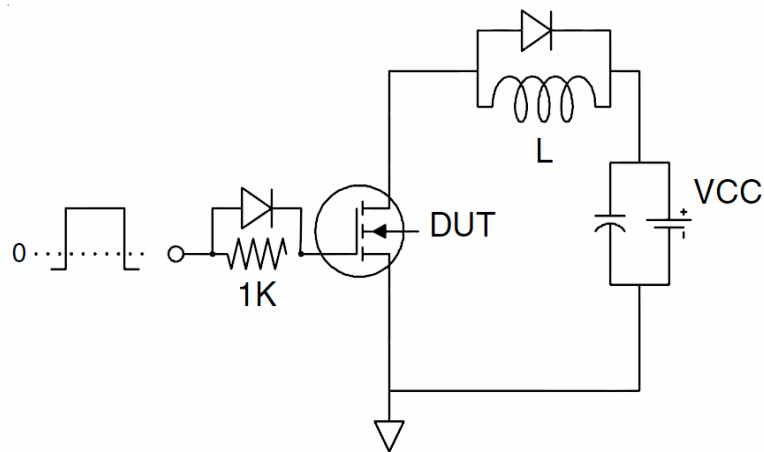
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test Circuit

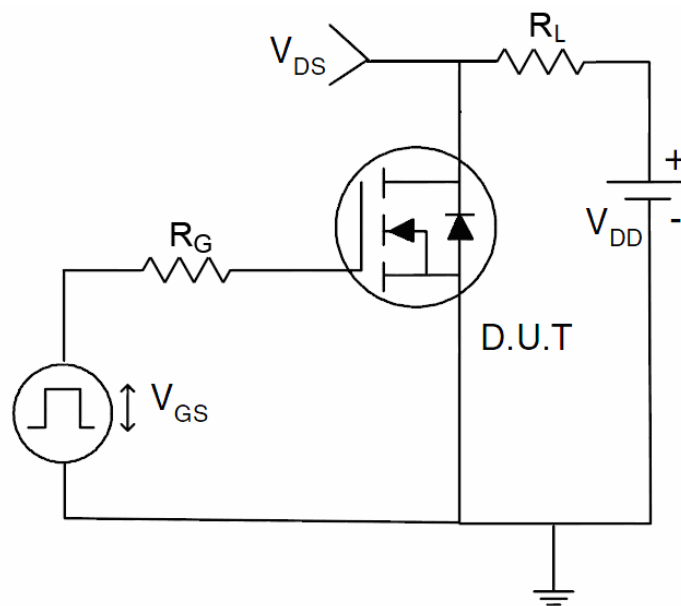
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

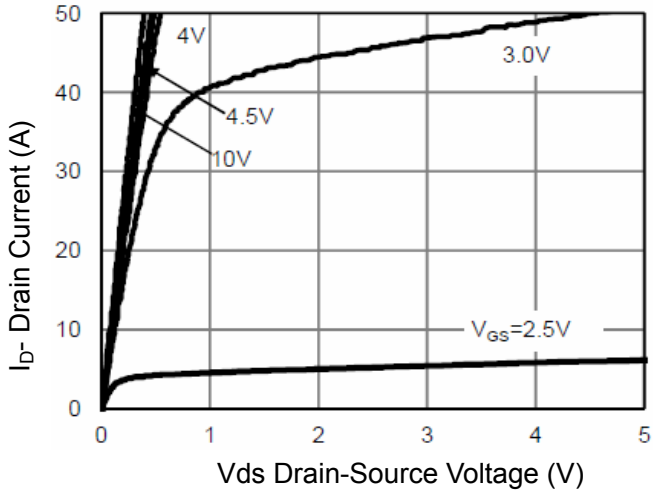


Figure 1 Output Characteristics

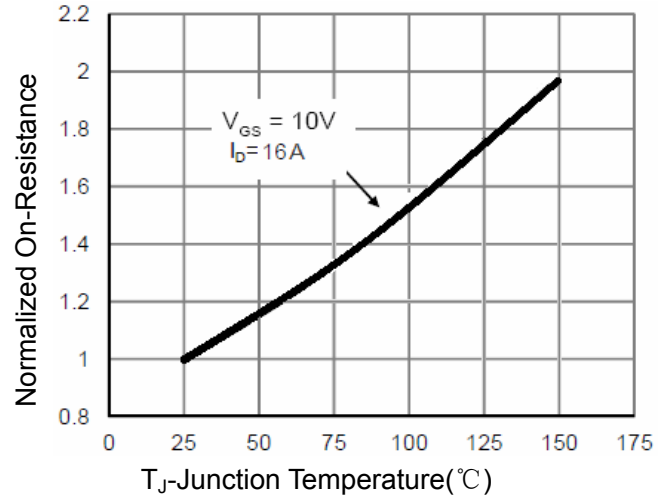


Figure 4 Rds(on)-Junction Temperature

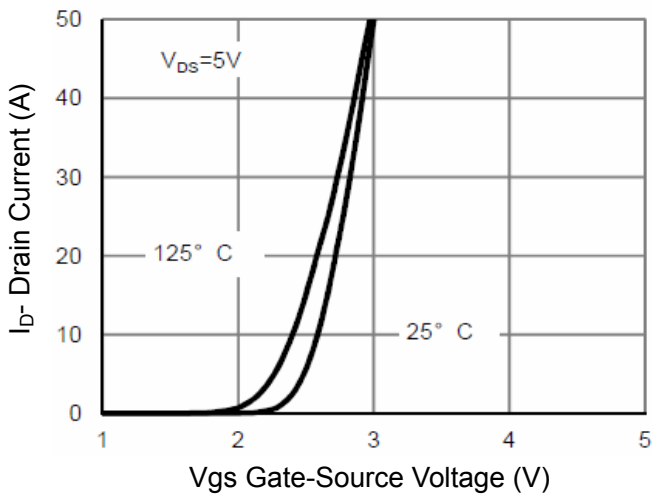


Figure 2 Transfer Characteristics

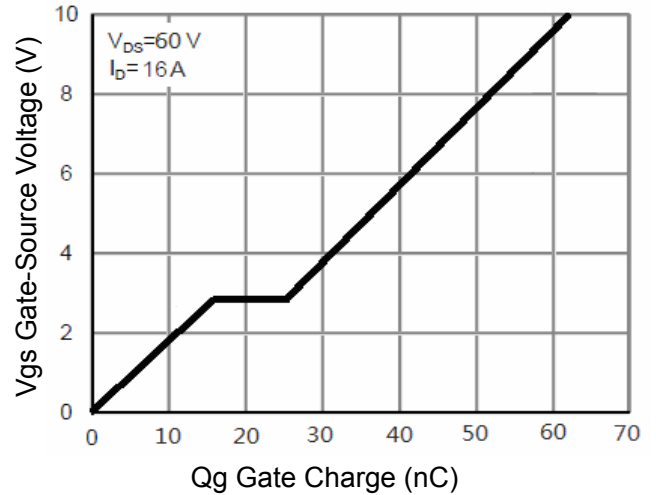


Figure 5 Gate Charge

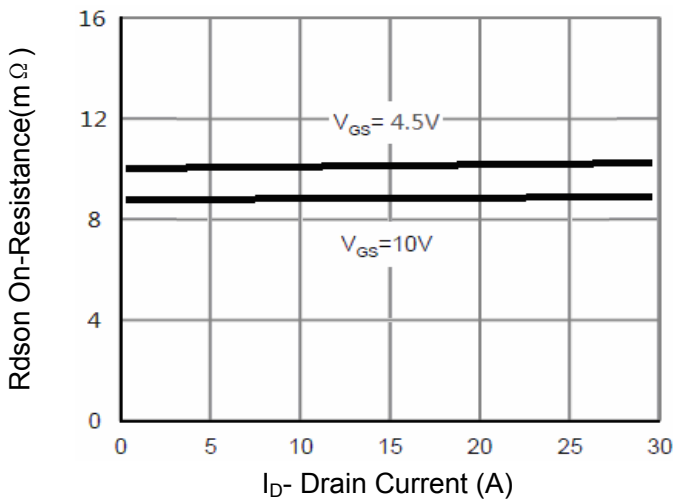


Figure 3 Rds(on)- Drain Current

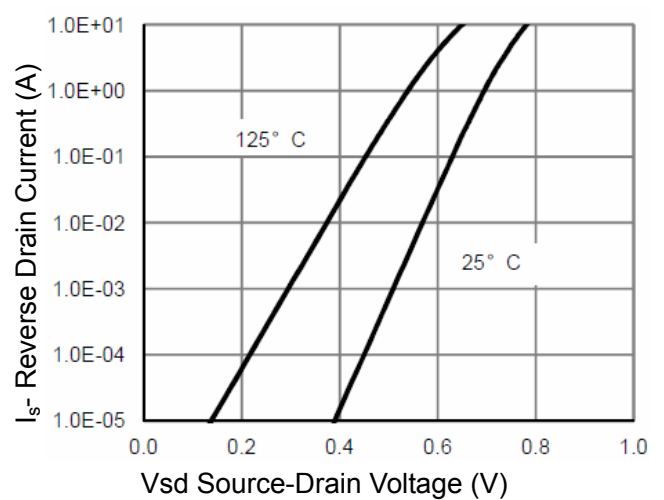


Figure 6 Source- Drain Diode Forward

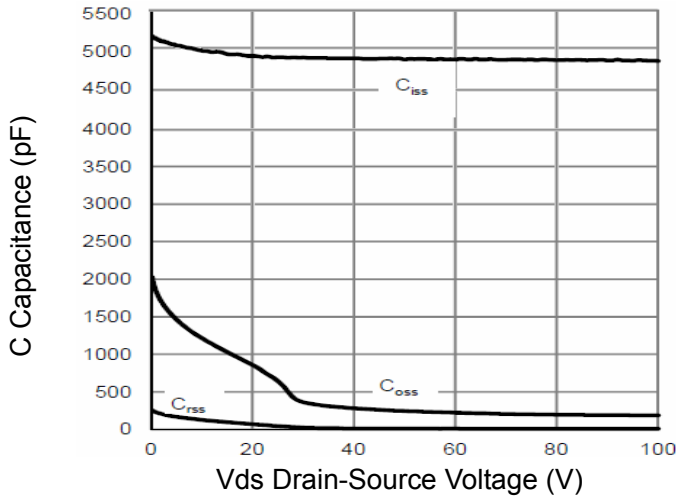


Figure 7 Capacitance vs Vds

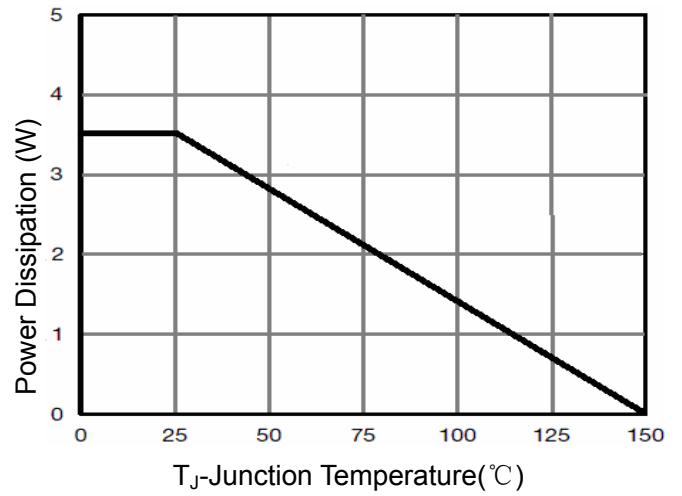


Figure 9 Power De-rating

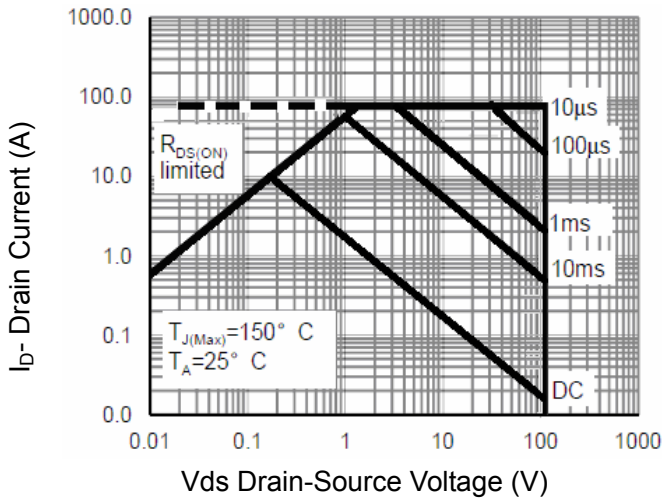


Figure 8 Safe Operation Area

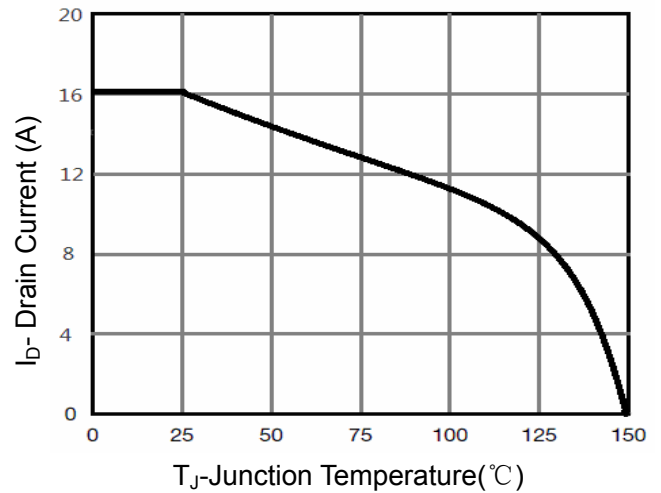


Figure 10 Current De-rating

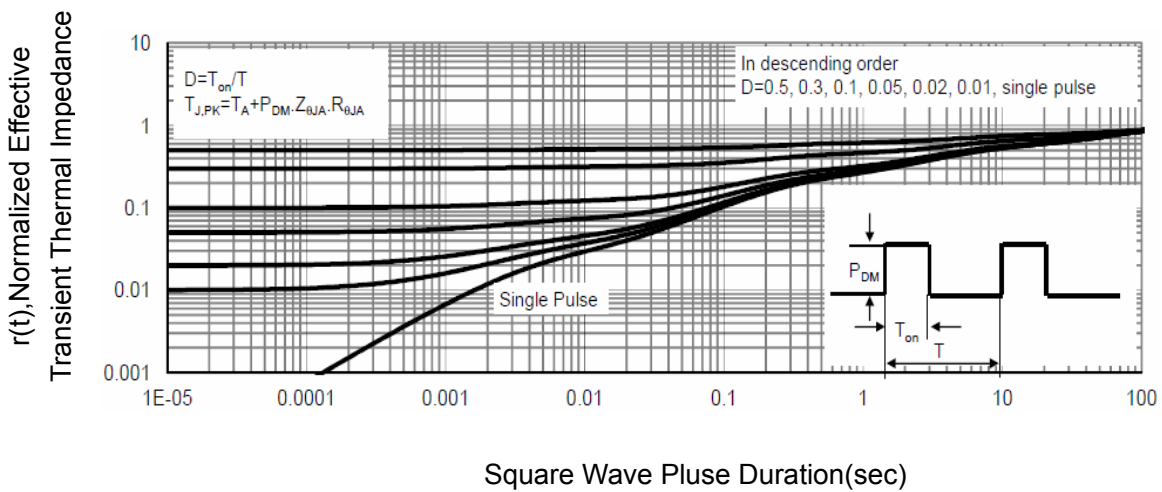
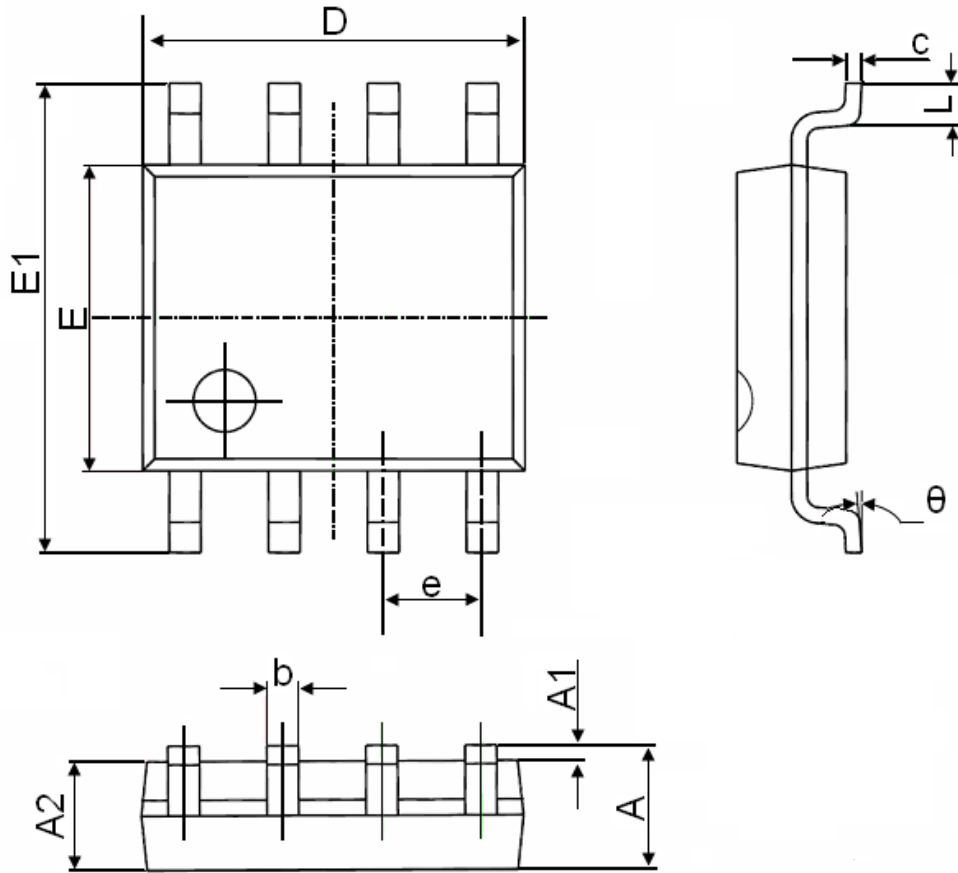


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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