

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE0117I uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

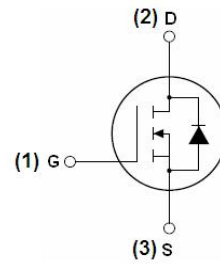
- $V_{DS} = 100V, I_D = 17A$
 $R_{DS(ON)} < 48m\Omega @ V_{GS} = 10V$ (Typ: 42m Ω)
 $R_{DS(ON)} < 53m\Omega @ V_{GS} = 4.5V$ (Typ: 44m Ω)
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits

100% UIS TESTED!

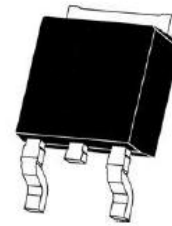
100% ΔV_{DS} TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE0117I	NCE0117I	TO-251	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	17	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	12	A
Pulsed Drain Current	I_{DM}	60	A
Maximum Power Dissipation	P_D	55	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	28	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	2.73	$^{\circ}C/W$
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Electrical Characteristics ($T_c=25^{\circ}C$ unless otherwise noted)

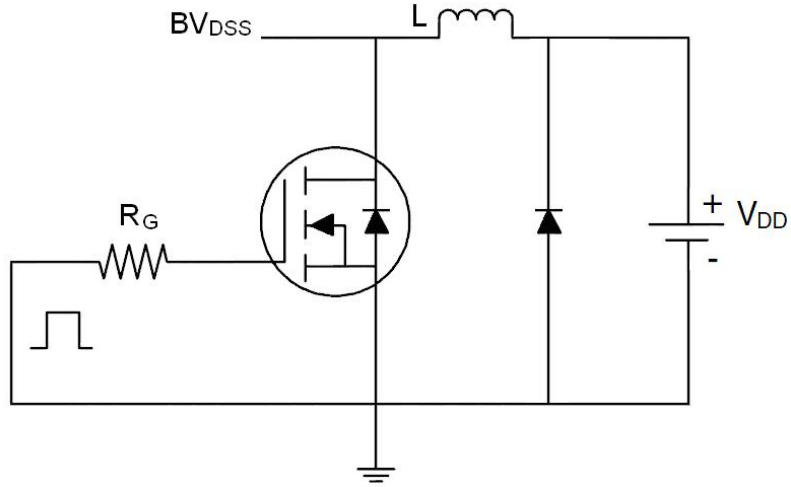
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$	-	42	48	m Ω
		$V_{GS}=4.5V, I_D=8A$	-	44	53	
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=10A$	-	14	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	1468	-	PF
Output Capacitance	C_{oss}		-	62	-	PF
Reverse Transfer Capacitance	C_{rss}		-	13.6	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	-	13.8	-	nS
Turn-on Rise Time	t_r		-	9.3	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	43.8	-	nS
Turn-Off Fall Time	t_f		-	11.4	-	nS
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=10A,$ $V_{GS}=10V$	-	40	-	nC
Gate-Source Charge	Q_{gs}		-	4.4	-	nC
Gate-Drain Charge	Q_{gd}		-	9.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=17A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	17	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

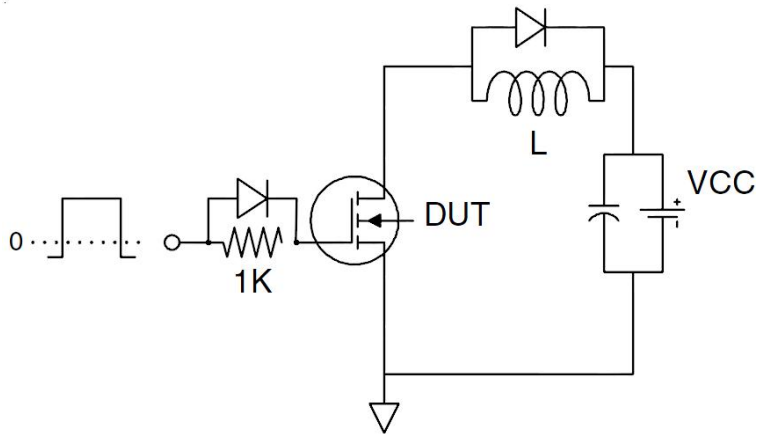
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_j=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

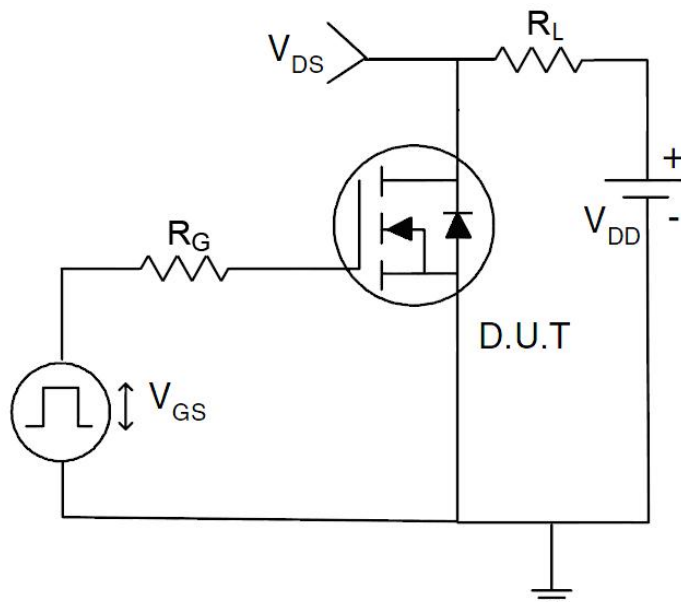
1) EAS test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

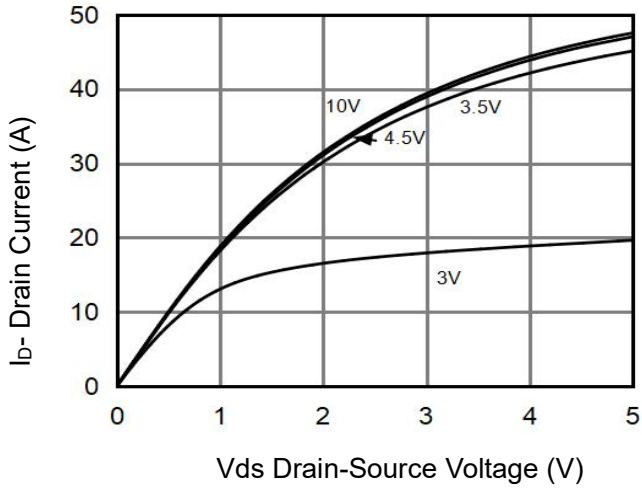


Figure 1 Output Characteristics

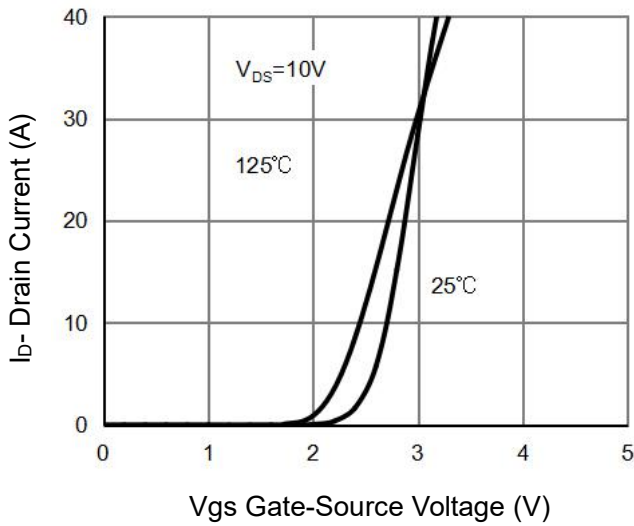


Figure 2 Transfer Characteristics

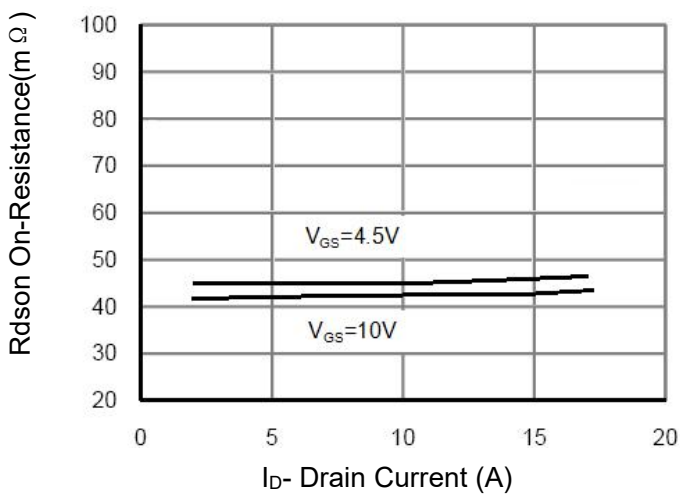


Figure 3 Rdson- Drain Current

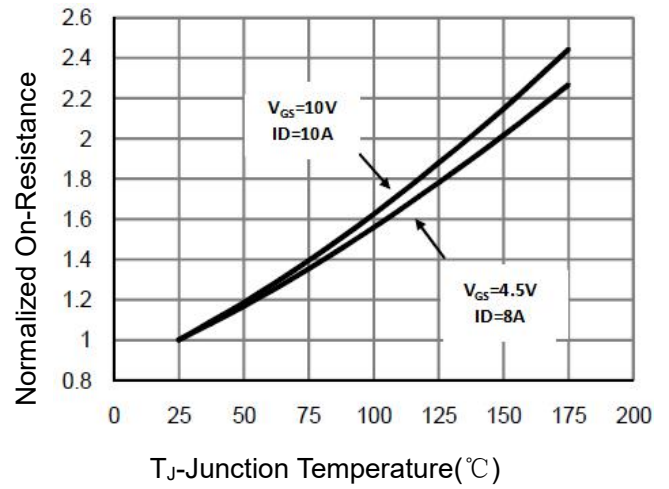


Figure 4 Rdson-Junction Temperature

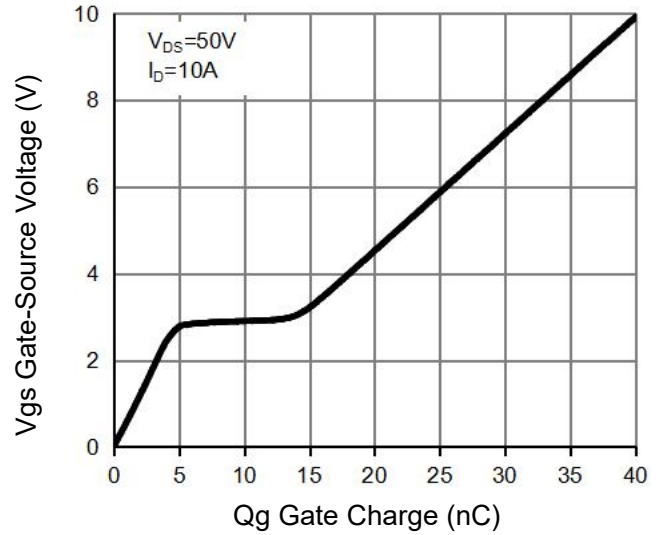


Figure 5 Gate Charge

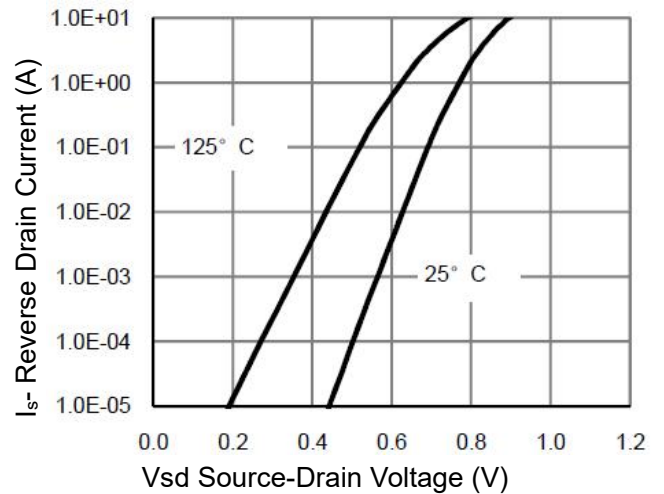


Figure 6 Source- Drain Diode Forward

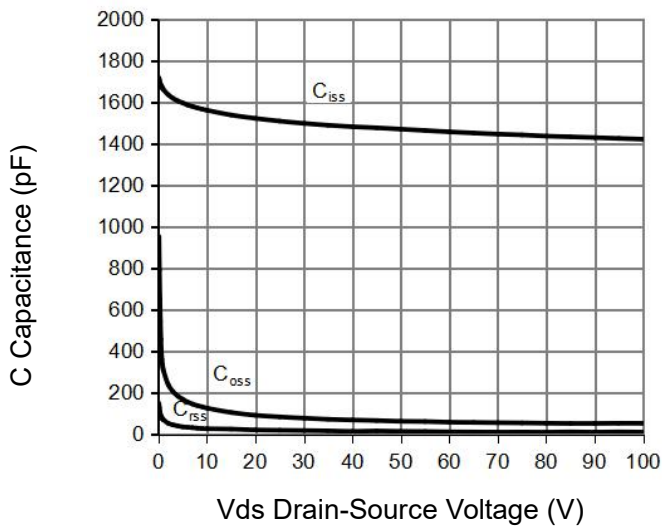


Figure 7 Capacitance vs Vds

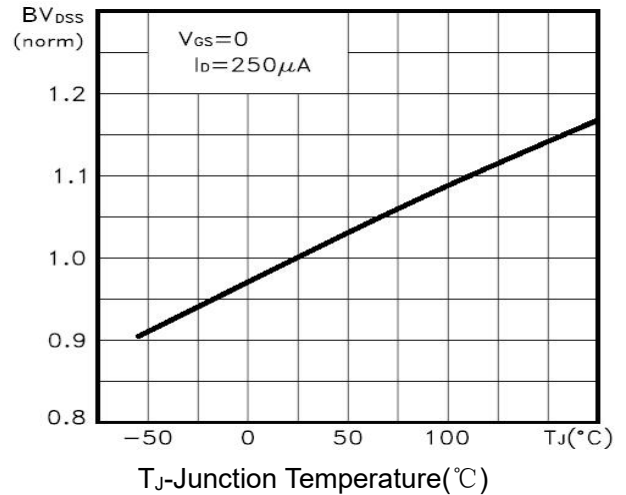


Figure 9 BV_{DSS} vs Junction Temperature

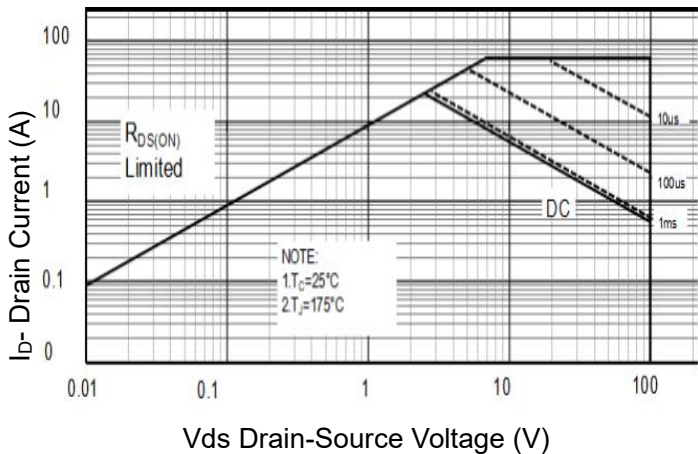


Figure 8 Safe Operation Area

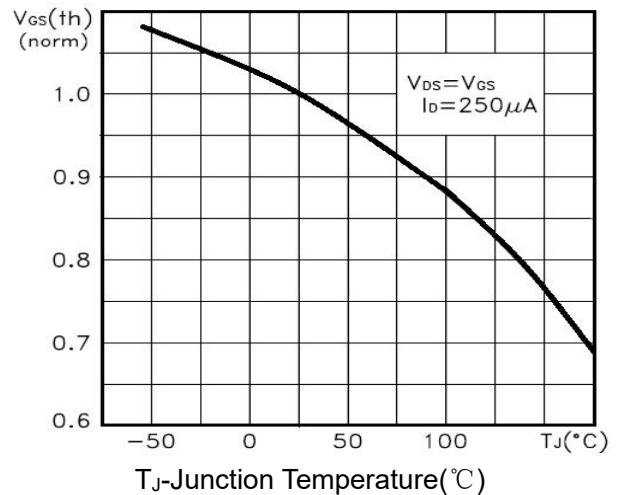


Figure 10 $V_{GS(th)}$ vs Junction Temperature

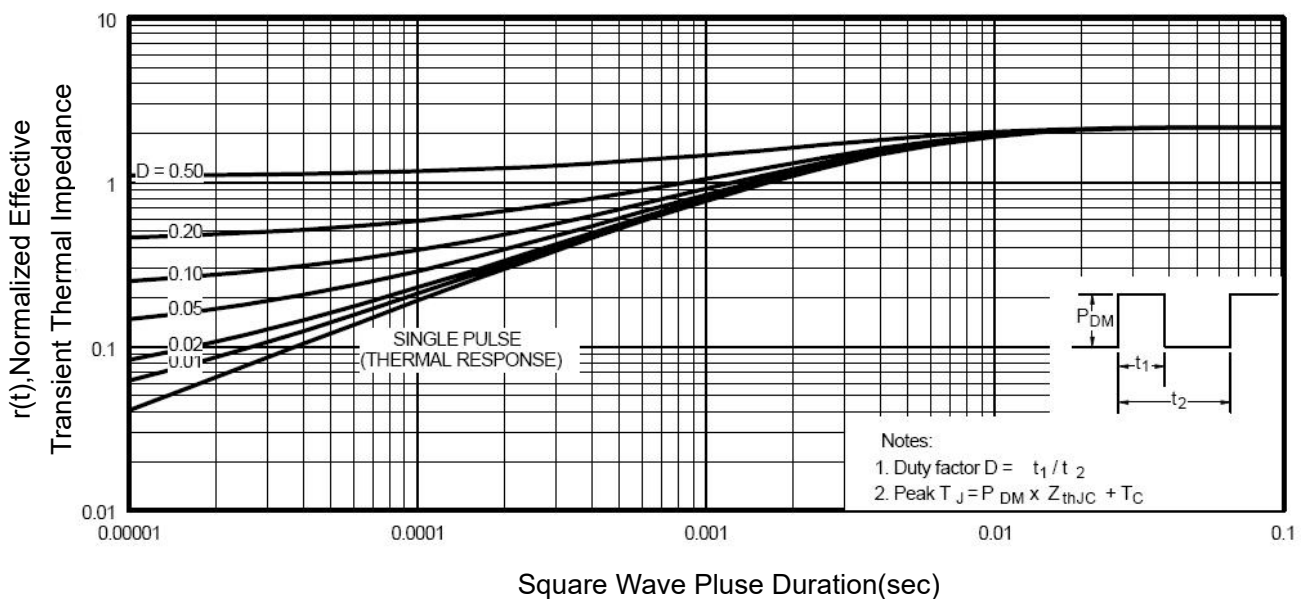
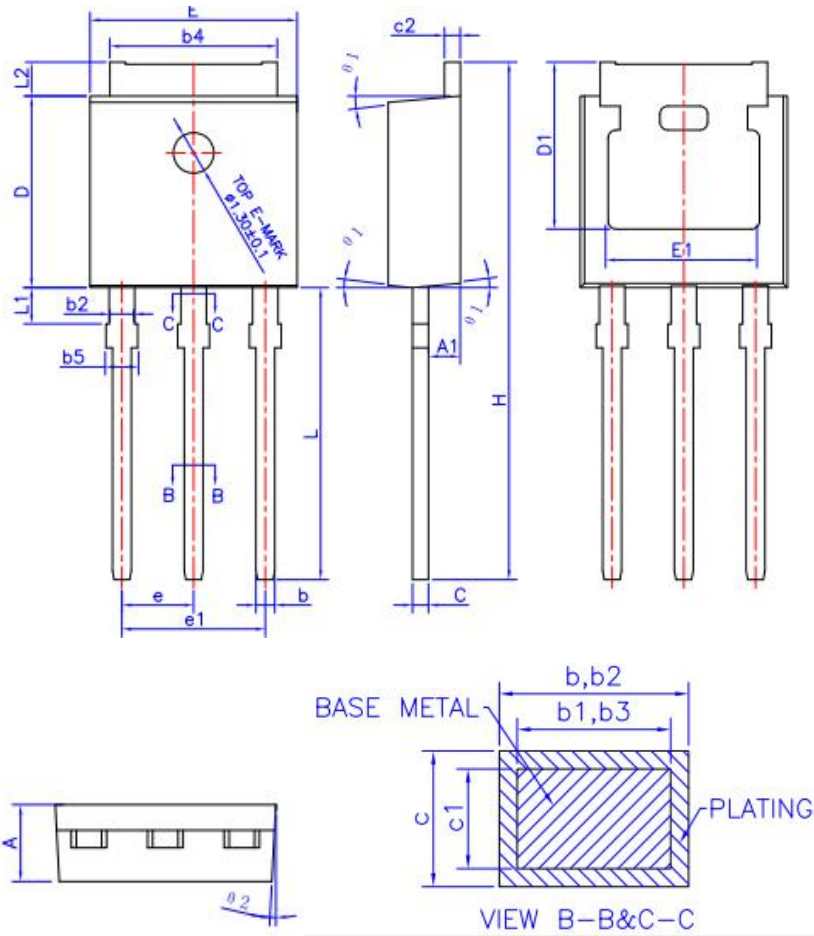


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252-2L Package Information



COMMON DIMENSIONS
(UNITS OF MEASURE =MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	2,20	2,30	2,35
A1	0,90	1,01	1,10
b	0,56	---	0,69
b1	0,55	0,60	0,65
b2	0,77	---	0,90
b3	0,76	0,81	0,86
b4	5,23	5,33	5,43
b5	---	---	1,05
c	0,46	---	0,59
c1	0,45	0,51	0,55
c2	0,46	---	0,59
D	6,00	6,10	6,20
D1	5,20	---	---
E	6,50	6,60	6,70
E1	4,60	4,83	5,00
e	2,24	2,29	2,34
e1	4,47	4,57	4,67
H	16,18	16,48	16,78
L	9,00	9,30	9,60
L1	0,95	1,16	1,35
L2	0,90	1,08	1,25
theta1	3°	5°	7°
theta2	1°	3°	5°

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