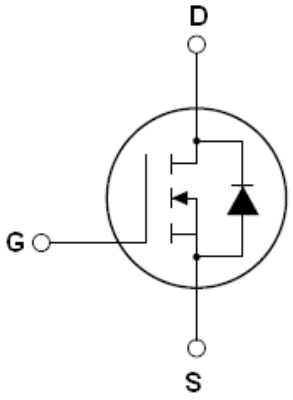
N-Channel Super Junction Power MOSFET Ⅲ

General Description

The series of devices use advanced super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

V_{DS}	650	V
$R_{DS(ON)\ TYP.}$	62	mΩ
I_D	53	A



Schematic diagram

Features

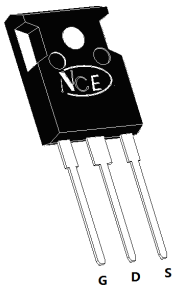
- New technology for high voltage device
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction（PFC）
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply（UPS）

Package Marking And Ordering Information

Device	Device Package	Marking
NCE65TF068T	TO-247	NCE65TF068T



TO-247

Table 1. Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (V_{GS}=0V)	V_{DS}	650	V
Gate-Source Voltage (V_{DS}=0V) AC (f>1 Hz)	V_{GS}	±30	V
Continuous Drain Current at Tc=25°C	$I_{D\ (DC)}$	53	A
Continuous Drain Current at Tc=100°C	$I_{D\ (DC)}$	33	A
Pulsed drain current **(Note 1)**	$I_{DM\ (pluse)}$	212	A
Maximum Power Dissipation(Tc=25℃) Derate above 25°C	P_D	435 3.48	W W/°C
Single pulse avalanche energy **(Note 2)**	E_{AS}	1440	mJ
Avalanche current **(Note 1)**	I_{AR}	24	A
Repetitive Avalanche energy , t_{AR} limited by T_{jmax} **(Note 1)**	E_{AR}	2	mJ

Parameter	Symbol	Value	Unit
Drain Source voltage slope, V_{DS} ≤480 V,	dv/dt	50	V/ns
Reverse diode dv/dt， V_{DS} ≤480 V,I_{SD}<I_D	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55...+150	°C

* limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance，Junction-to-Case（Maximum）	R_{thJC}	0.29	°C /W
Thermal Resistance，Junction-to-Ambient （Maximum）	R_{thJA}	62	°C /W

Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=500μA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	V_{DS}=650V,V_{GS}=0V			3	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I_{DSS}	V_{DS}=650V,V_{GS}=0V			300	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2.5	3.5	4.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=27A		62	78	mΩ
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=100V,V_{GS}=0V, F=1.0MHz		4070	4500	PF
Output Capacitance	C_{oss}			141		PF
Reverse Transfer Capacitance	C_{rss}			2.2		PF
Total Gate Charge	Q_g	V_{DS}=480V,I_D=53A, V_{GS}=10V		65	85	nC
Gate-Source Charge	Q_{gs}			22		nC
Gate-Drain Charge	Q_{gd}			17		nC
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=380V,I_D=27A, R_G=3.3Ω,V_{GS}=10V		28		nS
Turn-on Rise Time	t_r			19		nS
Turn-Off Delay Time	$t_{d(off)}$			98	160	nS
Turn-Off Fall Time	t_f			11	20	nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	T_C=25°C			53	A
Pulsed Source-drain current(Body Diode)	I_{SDM}				212	A
Forward on voltage	V_{SD}	Tj=25°C,I_{SD}=53A,V_{GS}=0V		0.9	1.3	V
Reverse Recovery Time	t_{rr}	Tj=25°C,I_F=27A,di/dt=100A/μs V_{DD}=300V		200		nS
Reverse Recovery Charge	Q_{rr}			2.5		uC
Peak Reverse Recovery Current	I_{rrm}			25		A

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. Tj=25℃,VDD=50V,VG=10V, R_G=25Ω

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe Operating Area

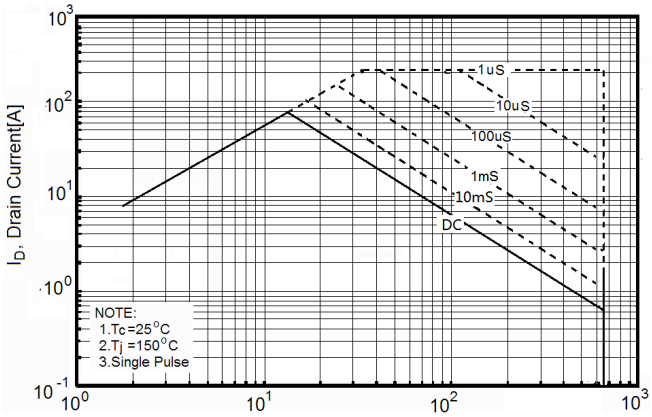


Figure3. Source-Drain Diode Forward Voltage

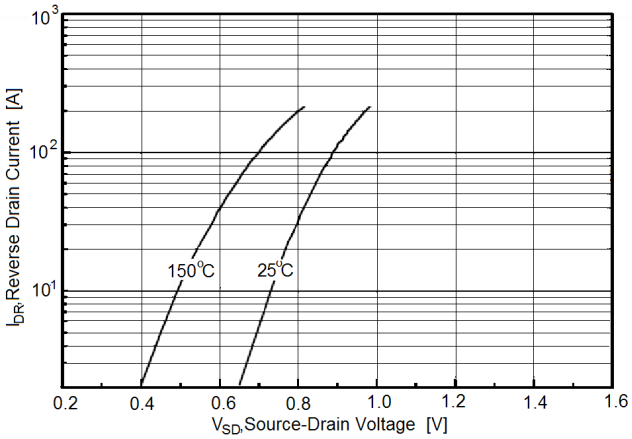


Figure4. Output Characteristics

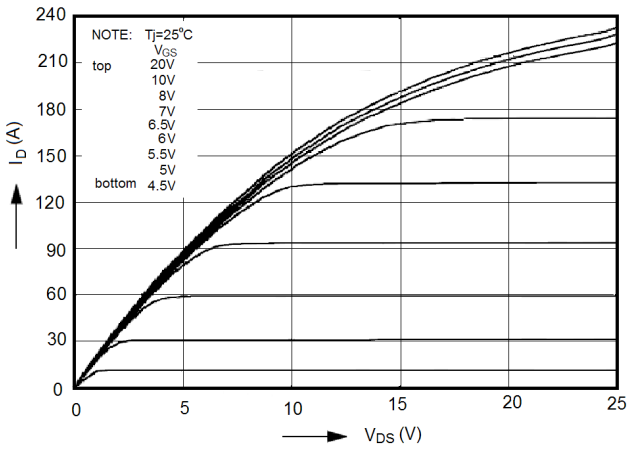


Figure5. Transfer Characteristics

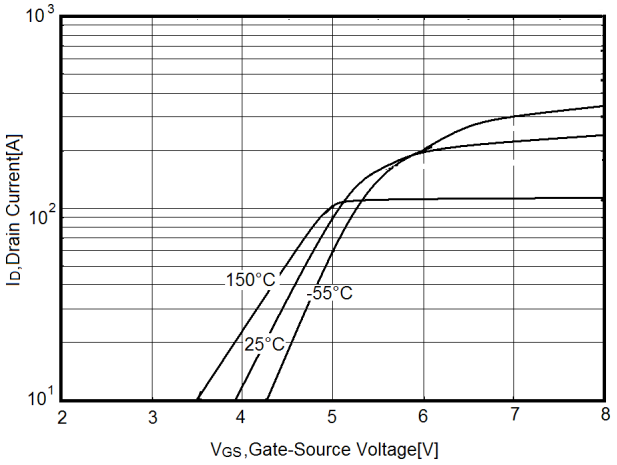


Figure6. Static drain-source on resistance

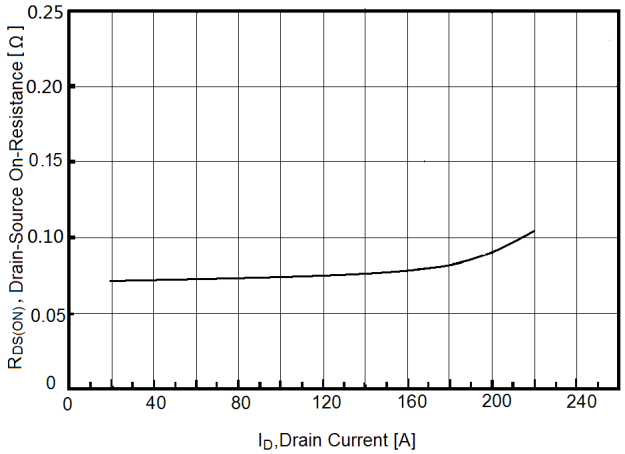


Figure7. $R_{DS(ON)}$ vs Junction Temperature

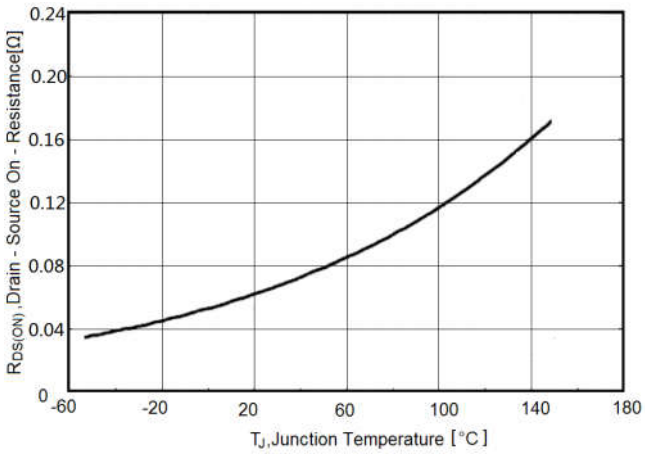


Figure8. BV_{DSS} vs Junction Temperature

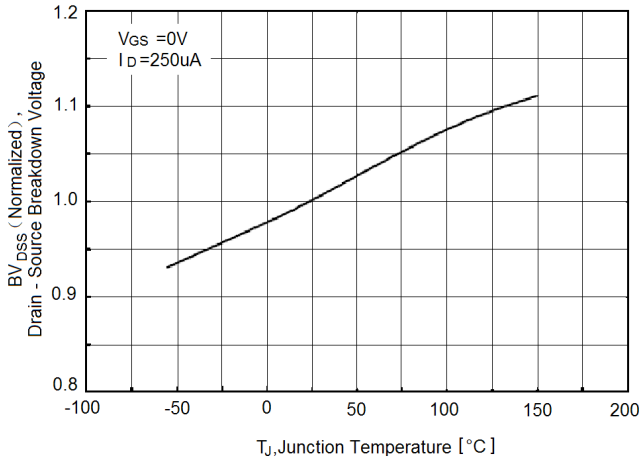


Figure9. Maximum I_D vs Junction Temperature

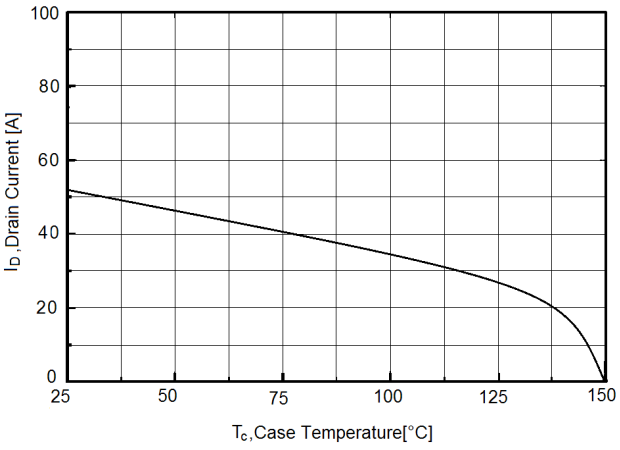


Figure10. Gate Charge Waveforms

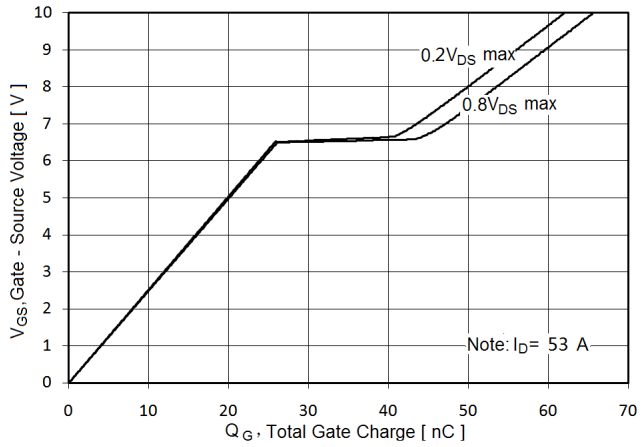
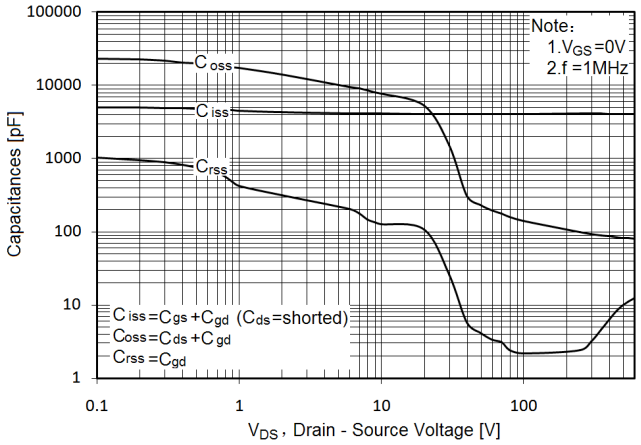
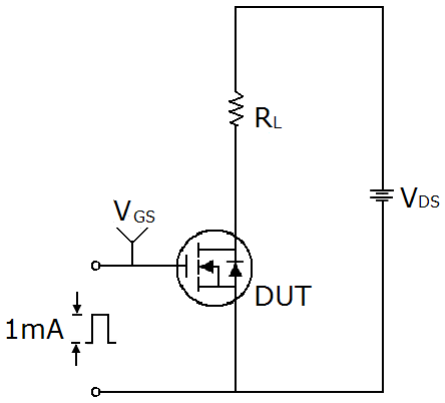


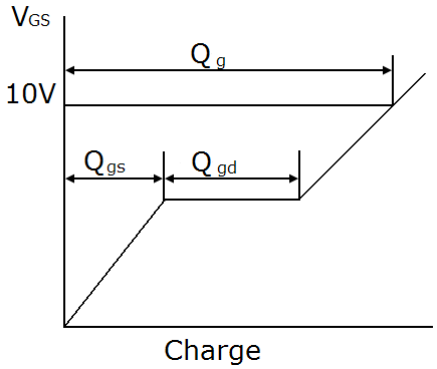
Figure11. Capacitance



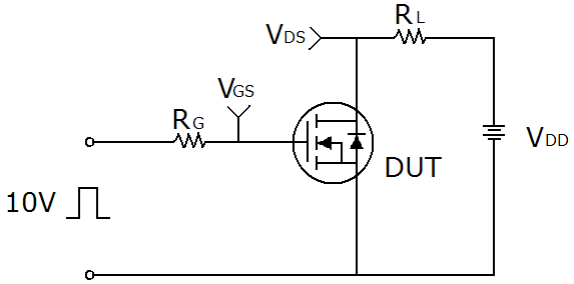
Test circuit

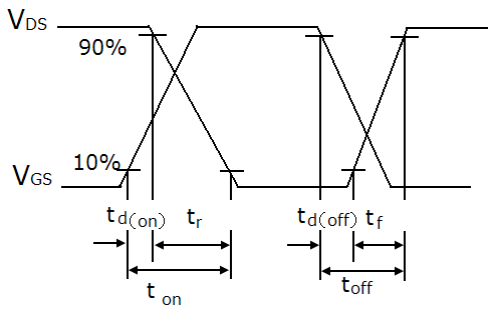
1）Gate charge test circuit & Waveform



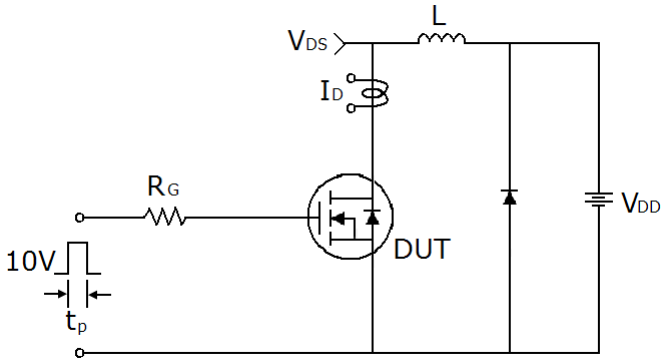


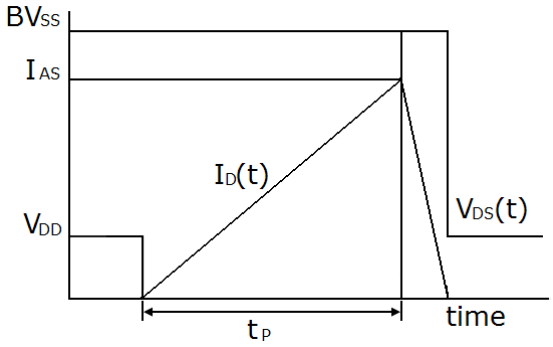
2）Switch Time Test Circuit:



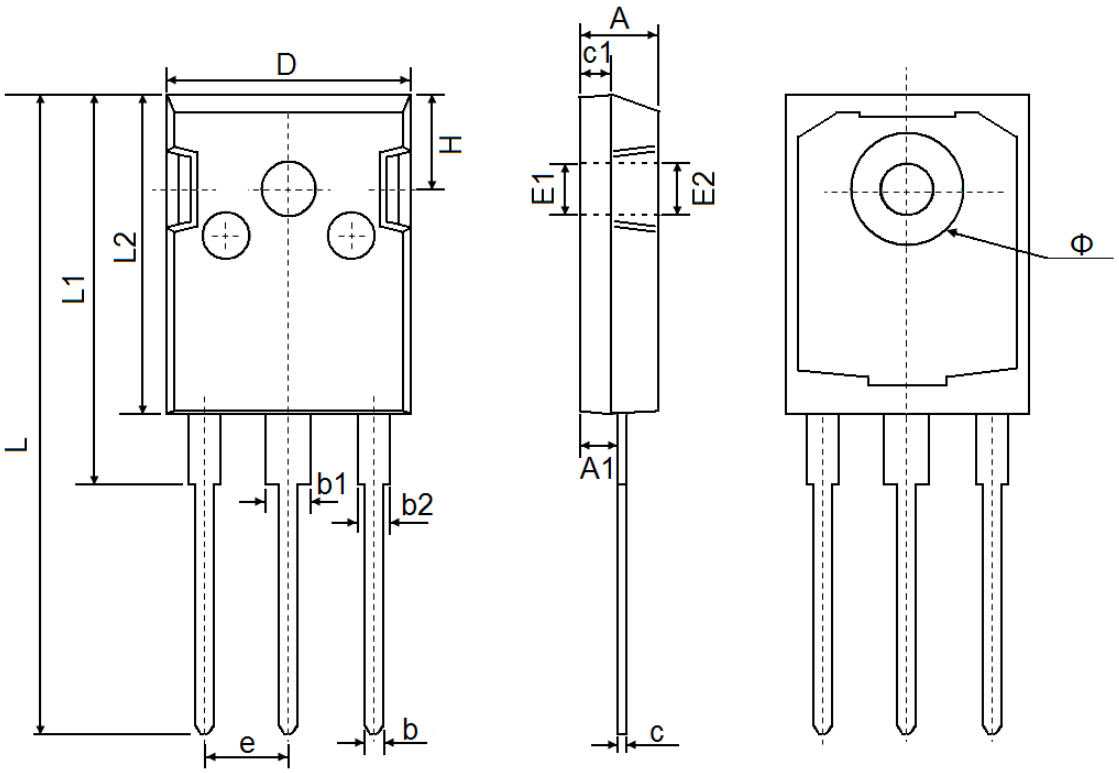


3）Unclamped Inductive Switching Test Circuit & Waveforms





TO-247 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
c	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500 REF		0.138 REF	
E2	3.600 REF		0.142 REF	
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
e	5.450 TYP		0.215 TYP	
H	5.980 REF		0.235 REF	

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